MODEL NAME : *QBLB0*

PCB NO : *LA-8381P*

BOM P/N : *4319H631L01 (Samsung 1G)*
4319H631L02(Samsung 2G)
4319H631L03(Hynix 1G)
4319H631L04(Hynix 2G)

Dell/Compal Confidential

Schematic Document

Specter MLK (Chief River)

Ivy Bridge(PGA) + Panther Point(standard)

DISCRETE VGA N13P-GT (optimus)

2011-10-26

Rev: X01

Highlight the short pad for 0 ohm

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Title: *Cover Page*

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Date: Thursday, January 12, 2012 Sheet 1 of 63

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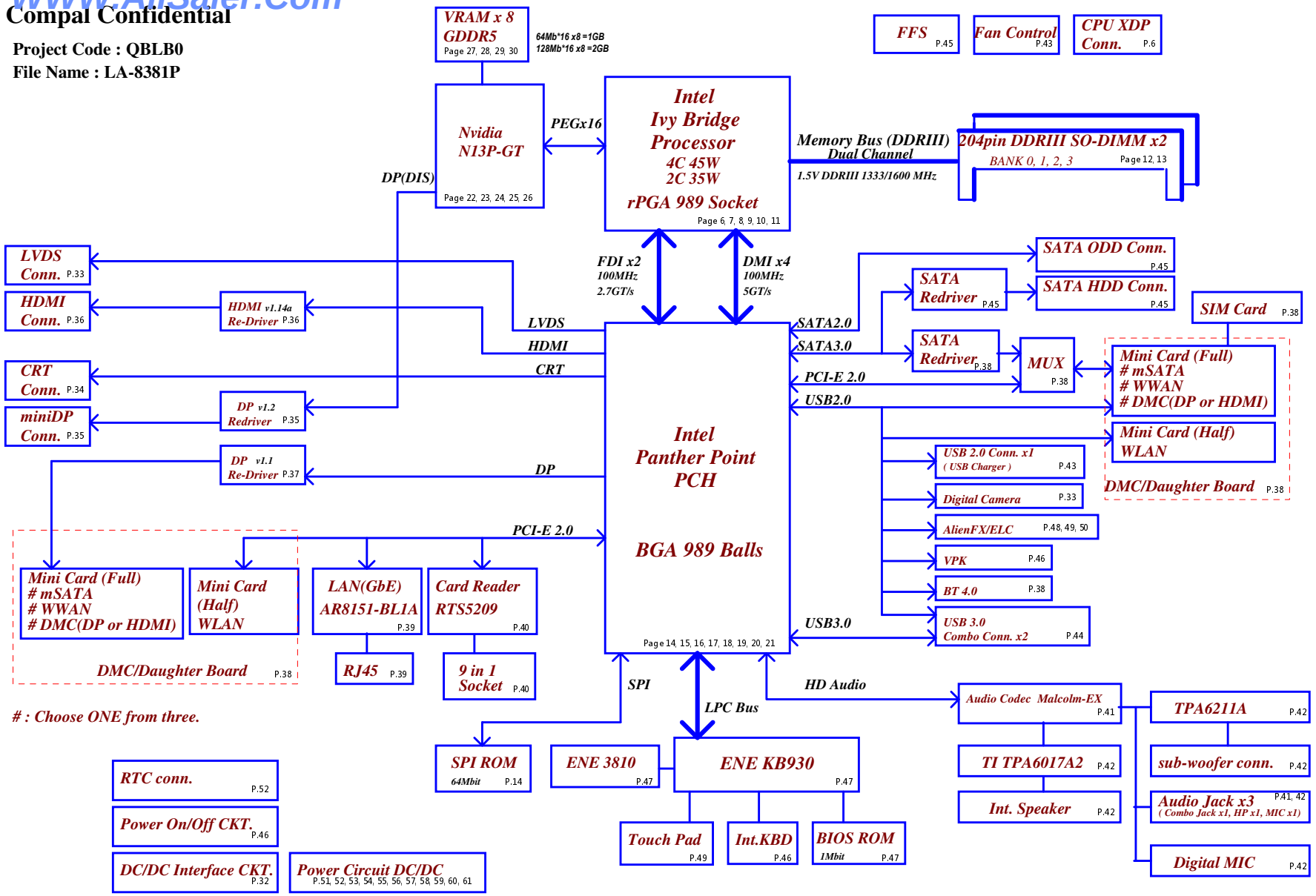
Project Code : QBLB0
File Name : LA-8381P



Security Classification	Compal Secret Data		
Issued Date	2011/02/23	Deciphered Date	2012/02/23

Compal Electronics, Inc.			
Title: Block Diagram			
Size	Document Number: LA-8381P		Rev: 1.0
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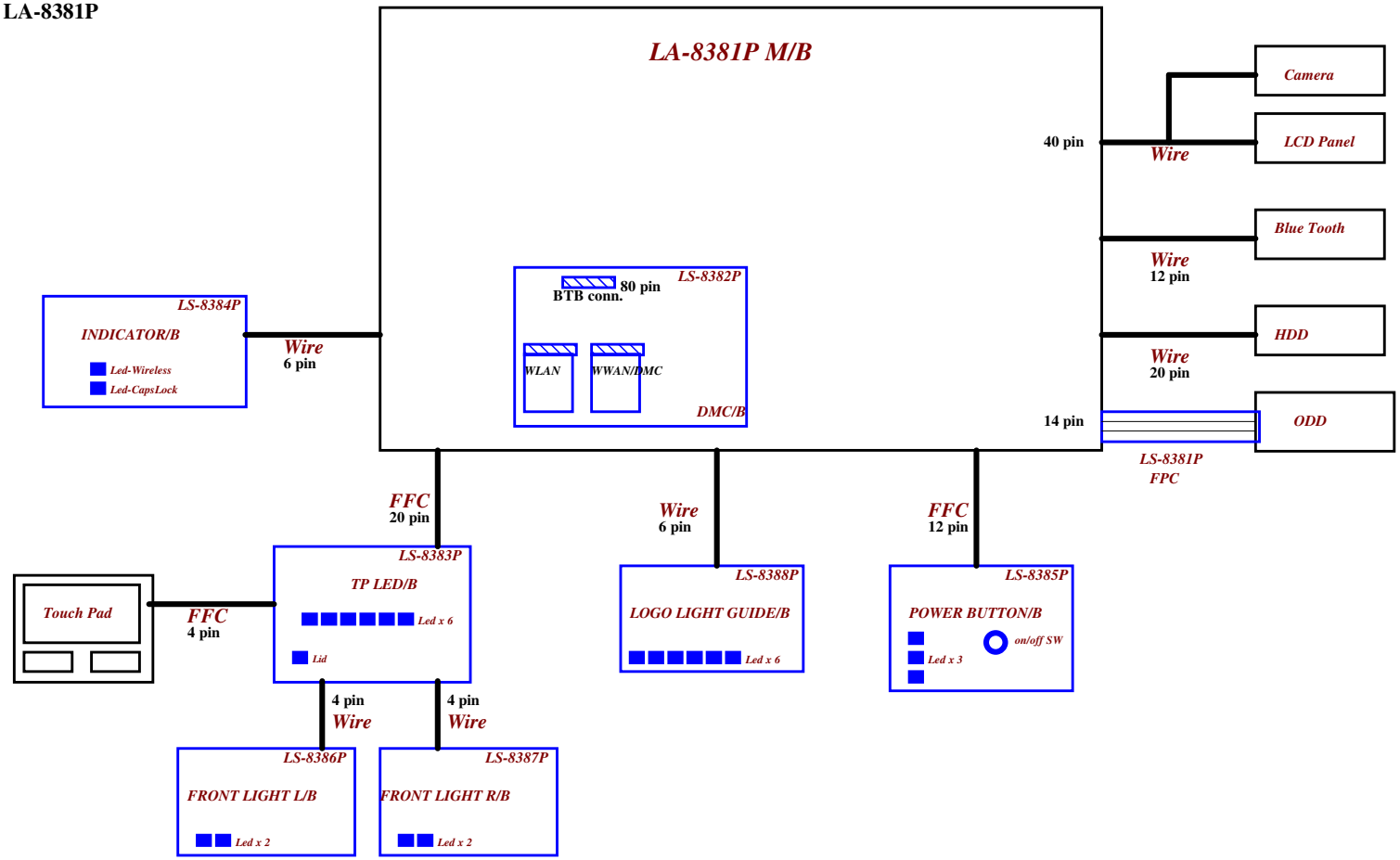
Project Code : QBLB0
File Name : LA-8381P



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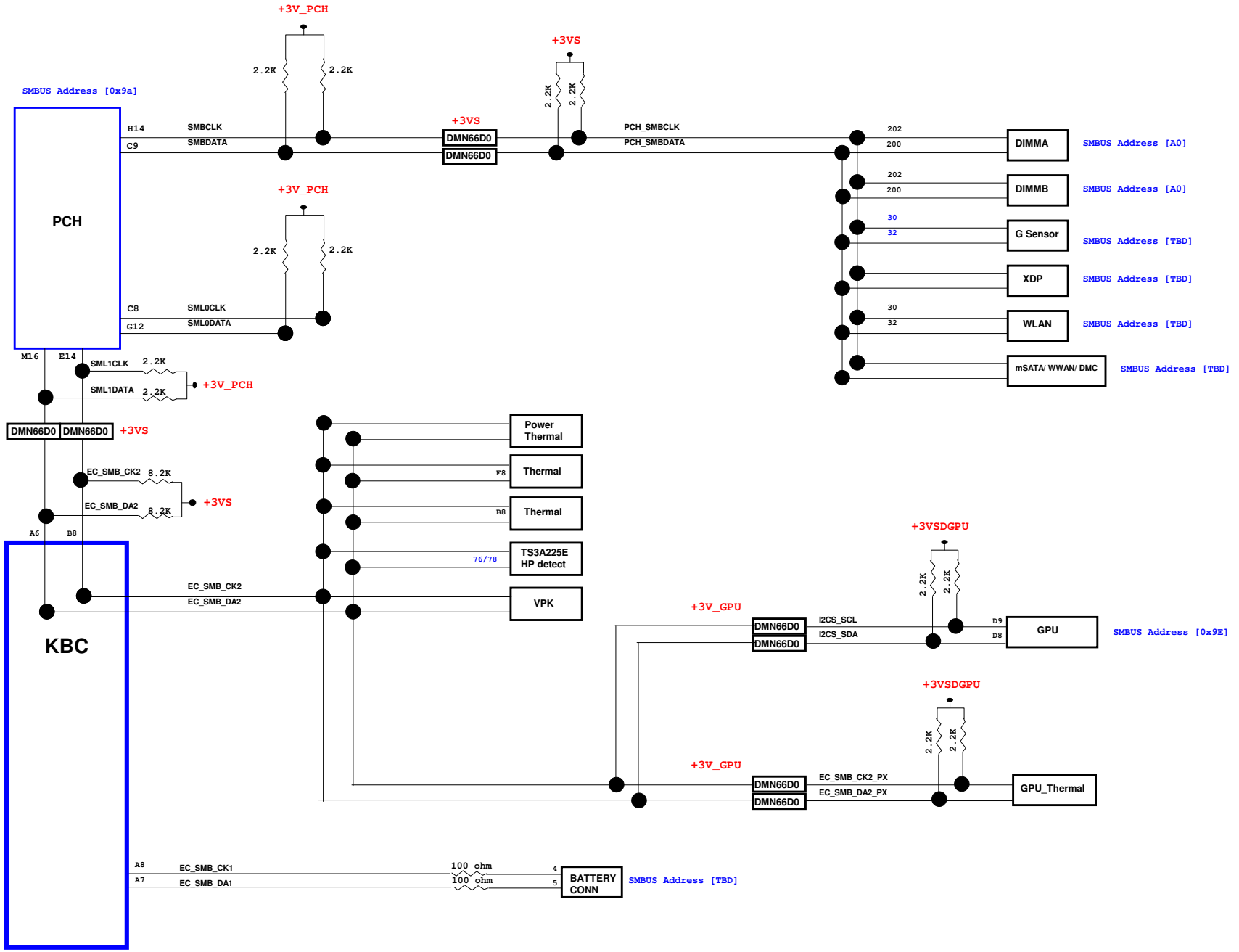
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.			
Title: Block Diagram			
Size	Document Number		Rev 1.0
Date: Thursday, January 12, 2012	Sheet 3 of 63		



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: Block Diagram

Size	Document Number	Rev
		1.0

Date: Thursday, January 12, 2012 Sheet 4 of 63

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID Table for AD channel

Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3	Board ID	PCB Revision
0	0	0 V	0 V	0.155 V	0x00-0x0C	0	
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C	1	
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30	2	
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49	3	
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69	4	SSI_X00
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E	5	PT_X01
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB	6	ST_X02
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF	7	QT_A00

BOARD ID Table

SMBUS Control Table

	SOURCE	MINI1 (WLAN)	MINI2 (DMC)	BATT	SODIMM	Thermal Sensor 1	Thermal Sensor 2	FFS	VGA Thermal Sensor	VGA	XDP	Charger	HP detect
EC_SMB_CK1 EC_SMB_DA1	KB930			V									
EC_SMB_CK2 EC_SMB_DA2	KB930					V	V		V	V		V	V
PCH_SML0CLK PCH_SML0DATA	PCH												
PCH_SML1CLK PCH_SML1DATA	PCH												
MEM_SMBCLK MEM_SMBDATA	PCH	V	V		V			V			V		

Link

PCH	USB PORT#	DESTINATION
	0	JUSB2 (v3.0 Ext Right Side)
	1	JUSB3 (v3.0 Ext Right side)
	2	None
	3	None
	4	JMINI1 (WLAN)
	5	JMINI2 (WWAN/DMC)
	6	ELC 8051
	7	None
	8	Bluetooth
	9	JUSB1 (2.0 Ext Left Side)
	10	None
	11	None
	12	CAMERA
	13	VPK

POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M-OFF	LOW	HIGH		HIGH	LOW	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

PM TABLE

power plane / State	+5VALW +3VALW +3VLP +3V_PCH	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.5V_CPU_VDDQ +VCCP = +1.05VS +VCC_CORE +VCC_GFXCORE_AXG +VCCSA +0.75VS +3VSDGPU +1.5VSDGPU +VGA_CORE
S0			
S3	ON	ON	ON
	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD-2 WWAN/DMC
Lane 3	MINI CARD-1 WLAN
Lane 4	CARD READER
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

CLK	DIFFERENTIAL	DESTINATION
	CLKOUT_PCIE0	None
	CLKOUT_PCIE1	10/100/1G LAN
	CLKOUT_PCIE2	MINI CARD-2 WWAN
	CLKOUT_PCIE3	MINI CARD-1 WLAN
	CLKOUT_PCIE4	CARD READER
	CLKOUT_PCIE5	None
	CLKOUT_PCIE6	None
	CLKOUT_PCIE7	None
	CLKOUT_PEG_B	None

FLEX CLOCKS	DESTINATION
CLKOUTFLEX0	None
CLKOUTFLEX1	None
CLKOUTFLEX2	None
CLKOUTFLEX3	None

Symbol Note :

: means Digital Ground

: means Analog Ground

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC LPC
PCI2	None
PCI3	None
PCI4	None

SATA	DESTINATION
SATA0	HDD
SATA1	m-SATA
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

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Title: Notes List

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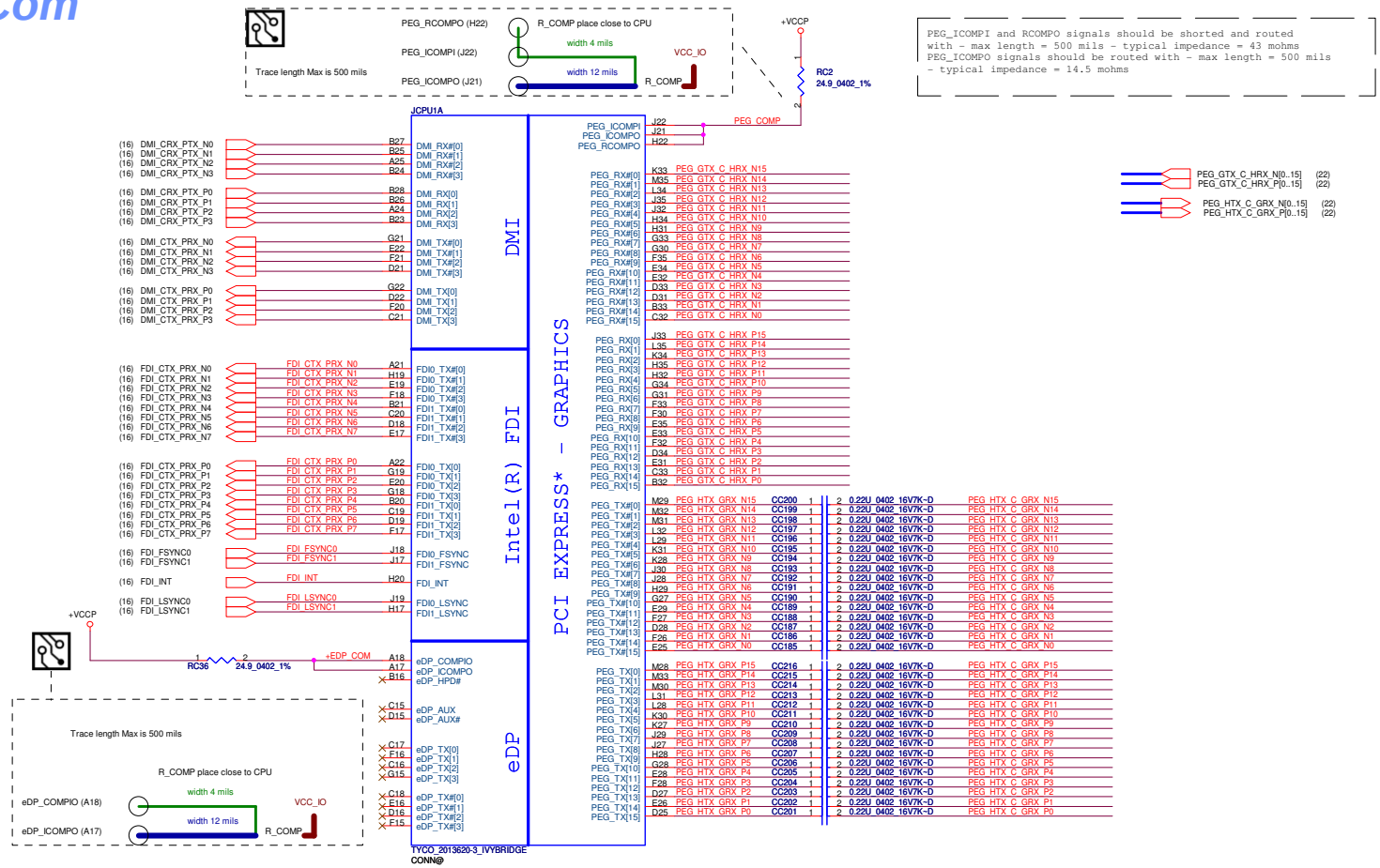
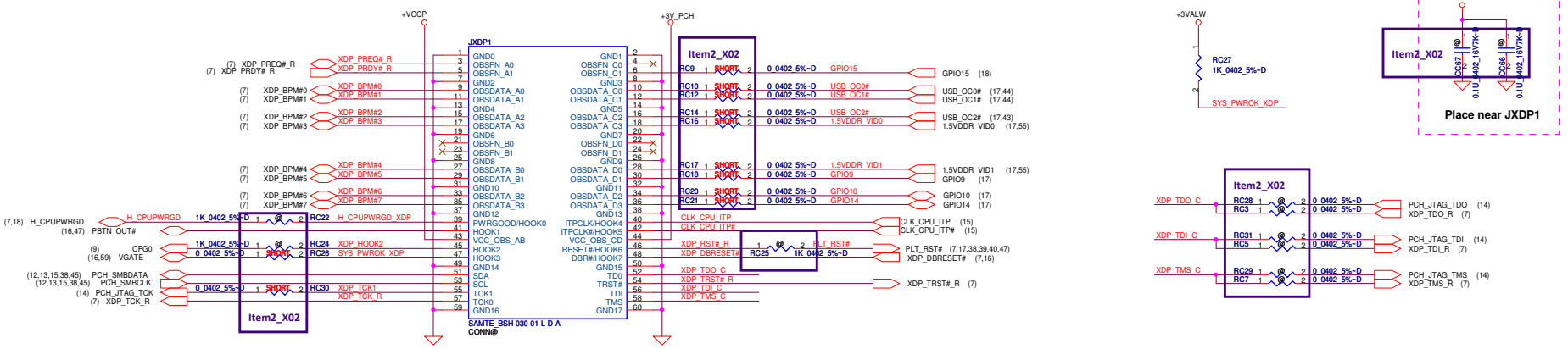


XDP Connector (Merged CPU-PCH)



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Compal Electronics, Inc.

Title: PROCESSOR(1/6) DMI,FDI,PEG

Size	Document Number	Rev
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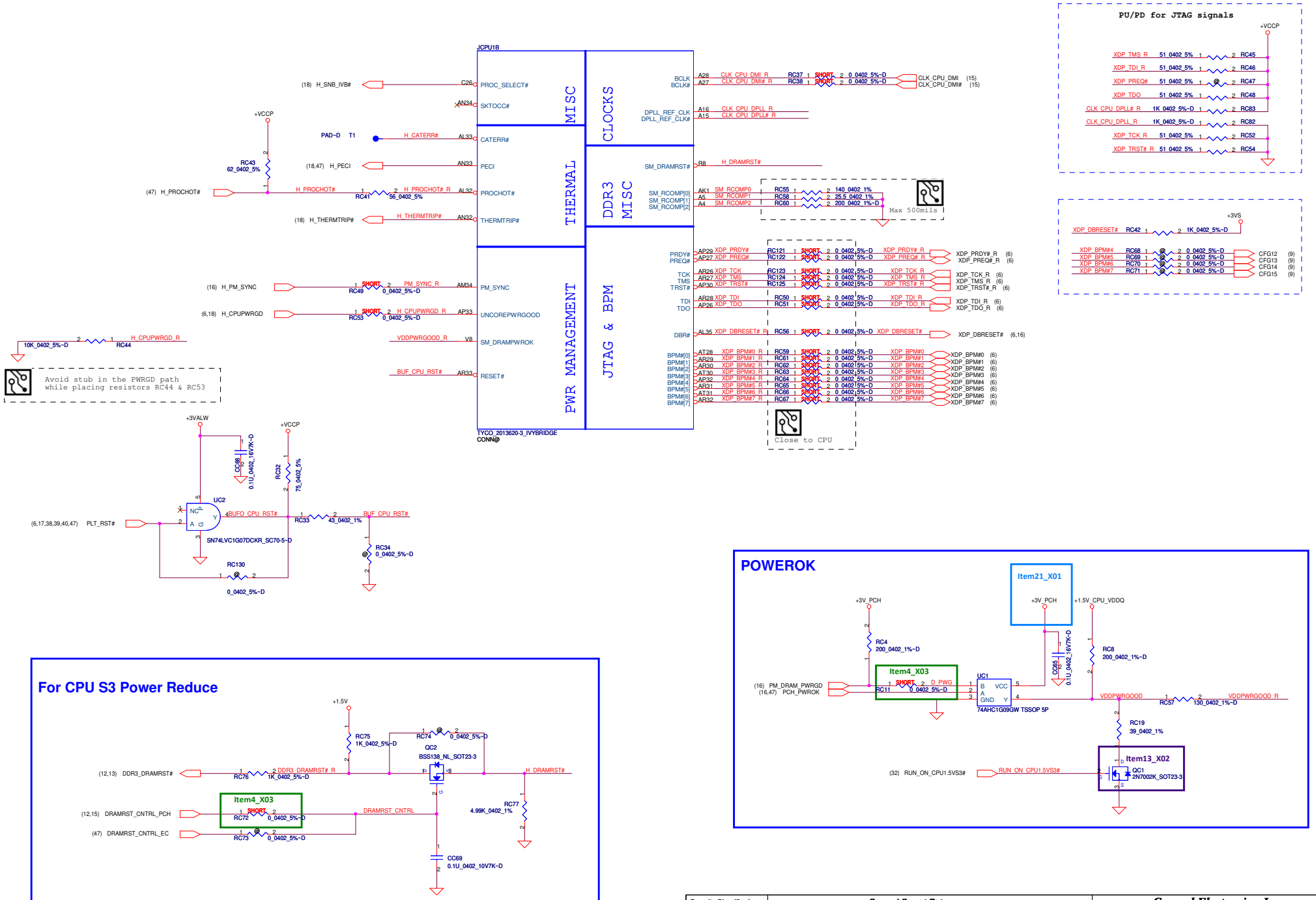
PM, XDP, CLK, S3 Reduce, PLTRST



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.			
Title	PROCESSOR(2/6) PM,XDP,CLK		
Size	Document Number		Rev
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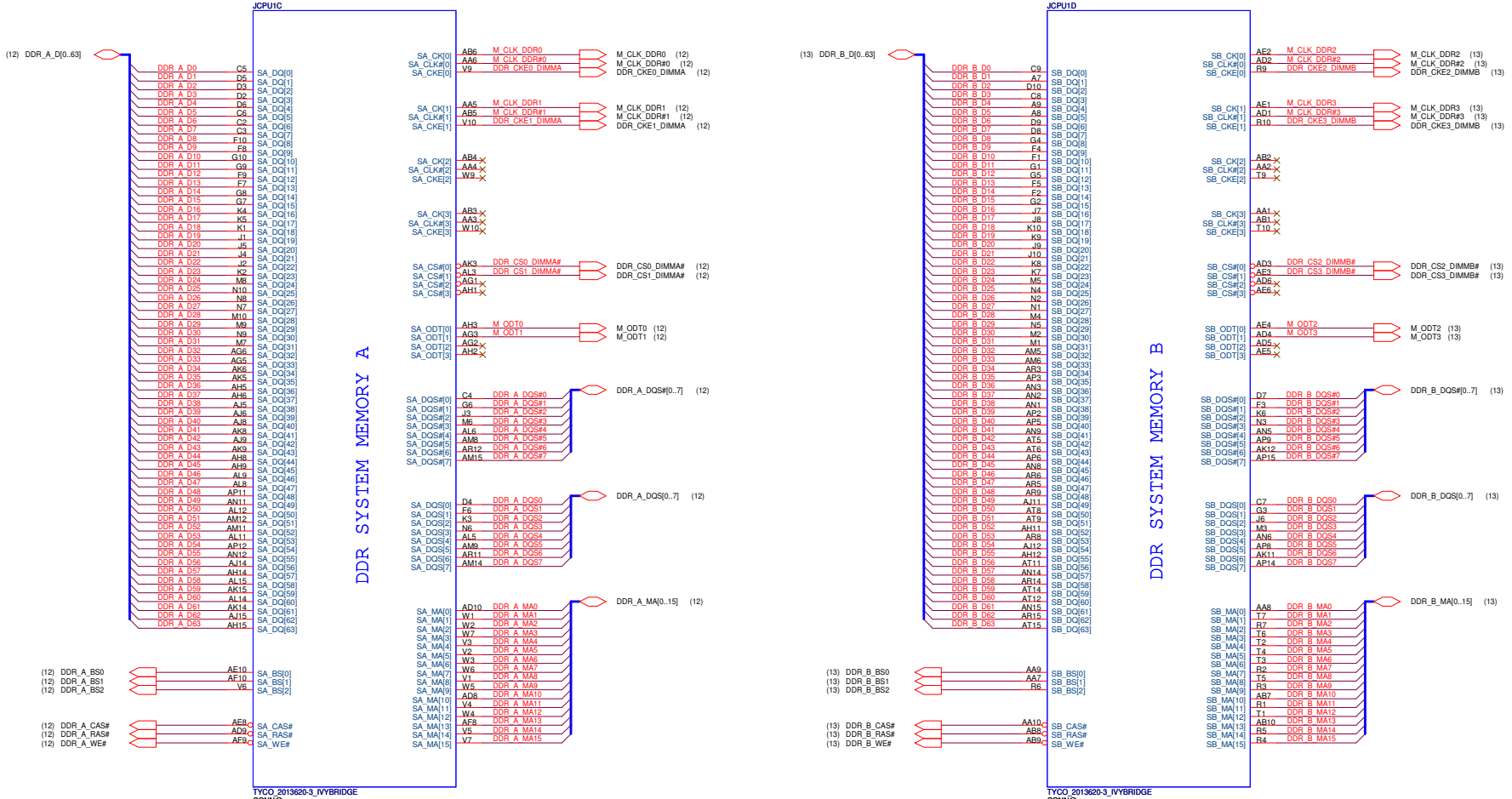

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.			
Title	PROCESSOR(3/6) DDRIII		
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CFG Straps for Processor

PEG Static Lane Reversal - CFG2 is for the 16x

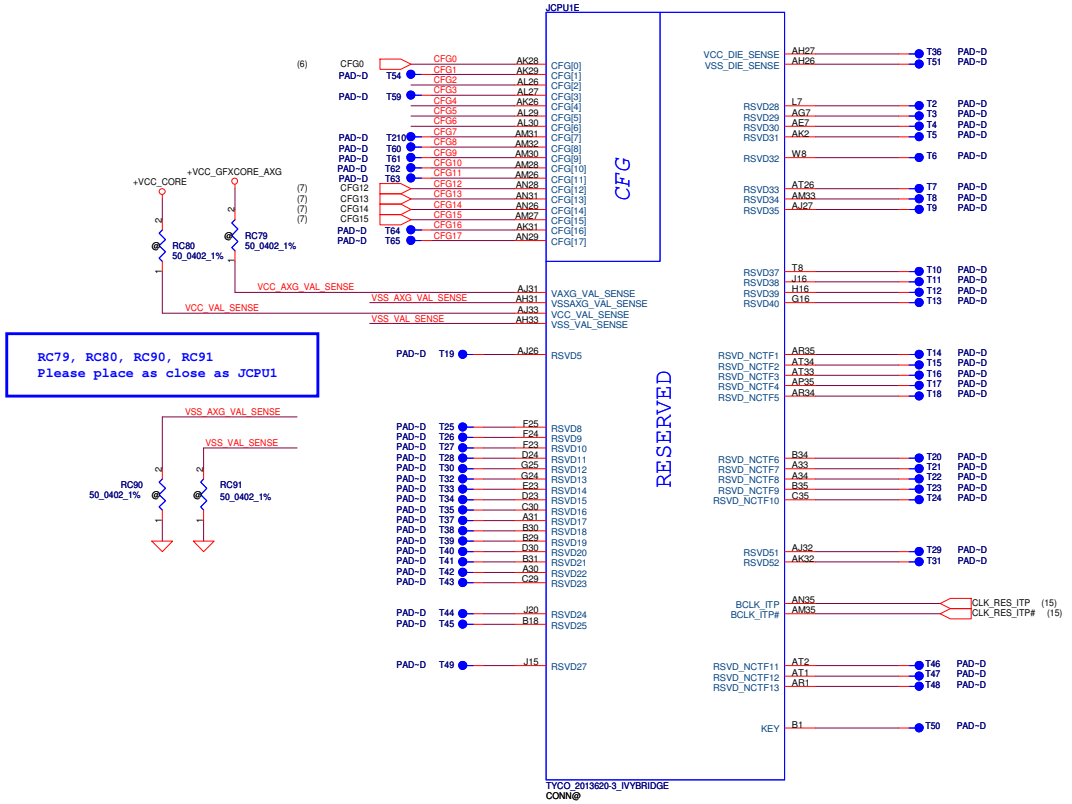
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed

Display Port Presence Strap

CFG4	* 1 :Disabled; No Physical Display Port attached to Embedded Display Port 0 :Enabled; An external Display Port device is connected to the Embedded Display Port

PCIE Port Bifurcation Straps

CFG[6:5]	*11:(Default) x16 - Device 1 functions 1 and 2 disabled 10:x8, 8 - Device 1 function 1 enabled ;function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: PROCESSOR(4/6) RSVD,CFG

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POWER

JCPU1F

QC=94A
DC=53A

+VCC_CORE

CORE SUPPLY

AG35 VCC1
AG34 VCC2
AG33 VCC3
AG32 VCC4
AG31 VCC5
AG30 VCC6
AG29 VCC7
AG28 VCC8
AG27 VCC9
AG26 VCC10
AF35 VCC11
AF34 VCC12
AF33 VCC13
AF32 VCC14
AF31 VCC15
AF30 VCC16
AF29 VCC17
AF28 VCC18
AF27 VCC19
AF26 VCC20
AE35 VCC21
AE34 VCC22
AE33 VCC23
AE32 VCC24
AE31 VCC25
AE30 VCC26
AD29 VCC27
AD28 VCC28
AD27 VCC29
AD26 VCC30
AC35 VCC31
AC34 VCC32
AC33 VCC33
AC32 VCC34
AC31 VCC35
AC30 VCC36
AC29 VCC37
AC28 VCC38
AC27 VCC39
AC26 VCC40
AA35 VCC41
AA34 VCC42
AA33 VCC43
AA32 VCC44
AA31 VCC45
AA30 VCC46
AA29 VCC47
AA28 VCC48
AA27 VCC49
AA26 VCC50
Y35 VCC51
Y34 VCC52
Y33 VCC53
Y32 VCC54
Y31 VCC55
Y30 VCC56
Y29 VCC57
Y28 VCC58
Y27 VCC59
Y26 VCC60
V35 VCC61
V34 VCC62
V33 VCC63
V32 VCC64
V31 VCC65
V30 VCC66
V29 VCC67
V28 VCC68
V27 VCC69
V26 VCC70
U35 VCC71
U34 VCC72
U33 VCC73
U32 VCC74
U31 VCC75
U30 VCC76
U29 VCC77
U28 VCC78
U27 VCC79
U26 VCC80
R35 VCC81
R34 VCC82
R33 VCC83
R32 VCC84
R31 VCC85
R30 VCC86
R29 VCC87
R28 VCC88
R27 VCC89
R26 VCC90
P35 VCC91
P34 VCC92
P33 VCC93
P32 VCC94
P31 VCC95
P30 VCC96
P29 VCC97
P28 VCC98
P27 VCC99
P26 VCC100

TYCO_2013620-3_IVYBRIDGE
CONN@

PEG AND DDR

+VCCP

8.5A

VCCIO1 AH13
VCCIO2 AH10
VCCIO3 AG10
VCCIO4 AC10
VCCIO5 V10
VCCIO6 U10
VCCIO7 P10
VCCIO8 L10
VCCIO9 J14
VCCIO10 J13
VCCIO11 J12
VCCIO12 J11
VCCIO13 H14
VCCIO14 H12
VCCIO15 H11
VCCIO16 G14
VCCIO17 G13
VCCIO18 G12
VCCIO19 F14
VCCIO20 F13
VCCIO21 F12
VCCIO22 F11
VCCIO23 E14
VCCIO24 E12
VCCIO25 E11
VCCIO26 D14
VCCIO27 D13
VCCIO28 D12
VCCIO29 D11
VCCIO30 C14
VCCIO31 C13
VCCIO32 C12
VCCIO33 C11
VCCIO34 B14
VCCIO35 B12
VCCIO36 A14
VCCIO37 A13
VCCIO38 A12
VCCIO39 A11
VCCIO40 J23

+VCCSA

Socket Cavity Socket Edge

CC167 10U_0805_25V6K-D
CC168 10U_0805_25V6K-D
CC169 10U_0805_25V6K-D
CC170 10U_0805_25V6K-D
CC171 330U_D2_2VM_R6M-D

+1.8VS

Item4_X03
RC109 1 SHORT 2 0_0805_5%-D

+1.8VS_VCCPLL

Socket Edge

CC172 10U_0805_25V6K-D
CC174 1U_0402_6.3V6K-D
CC175 1U_0402_6.3V6K-D
CC176 330U_D2_2.5VM_R6M-D

+1.5V

+1.5V_CPU_VDDQ

J8 PAD-OPEN 4x4m
J8_OPEN

Socket Edge

CC160 10U_0805_25V6K-D
CC161 10U_0805_25V6K-D
CC162 10U_0805_25V6K-D
CC163 10U_0805_25V6K-D
CC164 10U_0805_25V6K-D
CC165 10U_0805_25V6K-D
CC166 330U_D2_2VM_R6M-D

18-mil witdh,and shoulde use differential routing with 7-milseparation.
Signals must have equal trace length within 25 mils and are to be routed using external layer and GND referencing (no split plane referencing). VSS_SENSE, VCC_SENSE are to use 25-mils separation from any other signal or rail.

+0.75VS

+V_SM_VREF

RC106 1 SHORT 2 0_0402_5%-D
Item3_X02
CC250 0.1U_0402_10V7K-D

1K_0402_5%-D RC112
1K_0402_5%-D RC116

+VCC_GFXCORE_AXG

VCC_AXG_SENSE RC131 1 2 100_0402_5%-D
VSS_AXG_SENSE RC132 1 2 100_0402_5%-D

SVID

VIDALERT# AJ29 H_CPU_SVIDALRT# RC93 1 2 75_0402_5% VR_SVID_ALRT# (59)
VIDSCLK AJ30 H_CPU_SVIDCLK RC94 1 2 43_0402_1% VR_SVID_CLK (59)
VIDSOUT AJ28 H_CPU_SVIDDAT RC92 1 SHORT 2 0_0402_5%-D VR_SVID_DAT (59)
RC96 1 SHORT 2 0_0402_5%-D
RC95 1 2 130_0402_1%-D +VCCP

Item3_X02

RC95 close to CPU

VIDALERT#
Connect one end of series-resistor 43±5% close to processor and pull-up to VCCIO through 75±5% on the other end of the series-resistor towards Intel MVP 7.

VIDSOUT:
Requires a pull-up to VCCIO through a pull-up resistor of 130 ±5% close to the processor, and a pull-up to VCCIO through a pull-up resistor of 130 ±5% close to Intel MVP 7.
VIDSCLK:
Required pull-up to VCCIO through 55 ±5% close to Intel IMVP 7.

18-mil witdh,and shoulde use differential routing with 7-milseparation.
Signals must have equal trace length within 25 mils and are to be routed using external layer and GND referencing (no split plane referencing). VSS_SENSE, VCC_SENSE are to use 25-mils separation from any other signal or rail.

VCC_SENSE & VSS_SENSE:
xxxxxx
100- ±1% pull-down to GND near processor

SENSE LINES

+VCC_CORE

VCC_SENSE AJ35 VCCSENSE_R RC97 1 2 100_0402_1%-D VCCSENSE (59)
VSS_SENSE AJ34 VSSSENSE_R RC98 1 SHORT 2 0_0402_5%-D VSSSENSE (59)
RC99 1 SHORT 2 0_0402_5%-D
RC100 1 2 100_0402_1%-D

+VCCP

VCCIO_SENSE B10 RC126 1 2 10_0402_1%-D VCCIO_SENSE (56)
VSS_SENSE_VCCIO A10 RC129 1 2 10_0402_1%-D VSSIO_SENSE (56)

Item3_X02

POWER

+VCC_GFXCORE_AXG

JCPU1G

33A

VAXG1 AT24
VAXG2 AT23
VAXG3 AT21
VAXG4 AT20
VAXG5 AT18
VAXG6 AT17
VAXG7 AR24
VAXG8 AR23
VAXG9 AR21
VAXG10 AR20
VAXG11 AR18
VAXG12 AR17
VAXG13 AP24
VAXG14 AP23
VAXG15 AP21
VAXG16 AP20
VAXG17 AP18
VAXG18 AP17
VAXG19 AN24
VAXG20 AN23
VAXG21 AN21
VAXG22 AN20
VAXG23 AN18
VAXG24 AN17
VAXG25 AM24
VAXG26 AM23
VAXG27 AM21
VAXG28 AM20
VAXG29 AM18
VAXG30 AM17
VAXG31 AL24
VAXG32 AL23
VAXG33 AL21
VAXG34 AL20
VAXG35 AK18
VAXG36 AL17
VAXG37 AK24
VAXG38 AK23
VAXG39 AK21
VAXG40 AK20
VAXG41 AK18
VAXG42 AK17
VAXG43 AJ24
VAXG44 AJ23
VAXG45 AJ21
VAXG46 AJ20
VAXG47 AJ18
VAXG48 AJ17
VAXG49 AH24
VAXG50 AH23
VAXG51 AH21
VAXG52 AH20
VAXG53 AH18
VAXG54 AH17

GRAPHICS

SENSE LINES

VAXG_SENSE AK35 VCC_AXG_SENSE VCC_AXG_SENSE (59)
VSSAXG_SENSE AK34 VSS_AXG_SENSE VSS_AXG_SENSE (59)

VREF

+V_SM_VREF should have 10 mil trace width

SM_VREF AL1 +V_SM_VREF

SA_DIMM_VREFDQ B4 +V_DDR_REFA_R +V_DDR_REFA_R (12)
SB_DIMM_VREFDQ D1 +V_DDR_REFB_R +V_DDR_REFB_R (12)

10mil .Spacing is 10mil

DDR3 -1.5V RAILS

5A

+1.5V_CPU_VDDQ

VDDQ1 AF7
VDDQ2 AF4
VDDQ3 AF1
VDDQ4 AC7
VDDQ5 AC4
VDDQ6 AC1
VDDQ7 Y7
VDDQ8 Y4
VDDQ9 Y1
VDDQ10 U7
VDDQ11 U4
VDDQ12 U1
VDDQ13 P7
VDDQ14 P4
VDDQ15 P1

+1.5V_CPU_VDDQ

CC182 2 1 0.1U_0402_10V7K-D
CC184 2 1 0.1U_0402_10V7K-D
CC181 2 1 0.1U_0402_10V7K-D
CC183 2 1 0.1U_0402_10V7K-D

+1.5V

SA RAIL

6A

+VCCSA

VCCSA1 M27
VCCSA2 M26
VCCSA3 L26
VCCSA4 J26
VCCSA5 J25
VCCSA6 J24
VCCSA7 H26
VCCSA8 H25

VCCSA_SEL Voltage Selection Table

VID[0] Pin AE10	VID[1] Pin AG10	VCCSA Vout
0	0	0.90 V
0	1	0.80 V
1	0	0.725 V
1	1	0.675 V

1.2A

+1.8VS_VCCPLL

TBD

VCCPLL1 B6
VCCPLL2 A6
VCCPLL3 A2

1.8V RAIL

MISC

VCCSA_SENSE H23 VCCSA_SENSE (57)

VCCSA_VID[0] C22 VCCSA_VID0 RC111 1 SHORT 2 0_0402_5%-D H_VCCSA_VID0 (57)
VCCSA_VID[1] C24 VCCSA_VID1 RC108 1 SHORT 2 0_0402_5%-D H_VCCSA_VID1 (57)

10mil .Spacing is 10mil

VCCIO_SEL A19 H_VCCP_SEL RC88 1 SHORT 2 0_0402_5%-D VCCP_PWRCTRL (56)

Item3_X02

Need PWR add new circuit on 1.05V(refer CRB)

TYCO_2013620-3_IVYBRIDGE
CONN@

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: PROCESSOR(5/6) PWR,BYPASS

Size	Document Number	Rev
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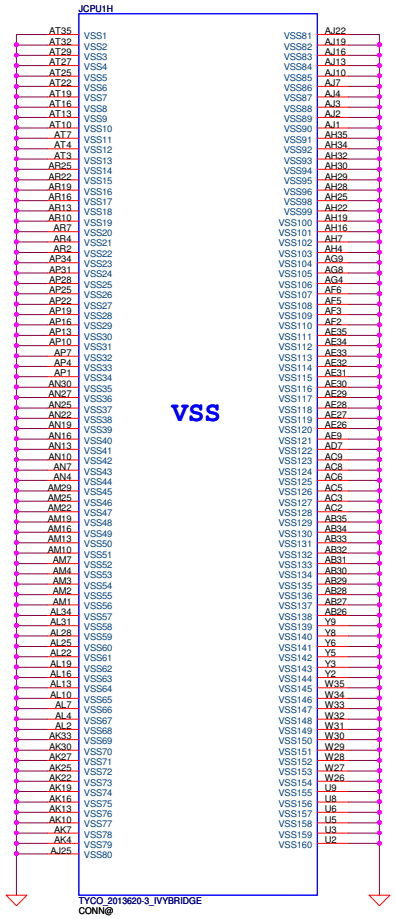

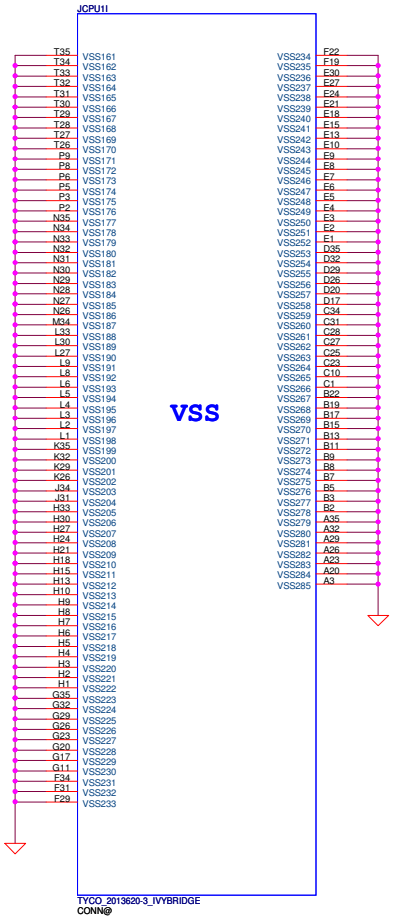

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.			
Title	PROCESSOR(6/6) PWR,VSS		
Size	Document Number		Rev
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(8) DDR_A_DQS#[0..7]
(8) DDR_A_DQS[0..7]
(8) DDR_A_D[0..63]
(8) DDR_A_MA[0..15]

All VREF traces should have 10 mil trace width

All VREF traces should have 10 mil trace width

+1.5V_SUS decoupling caps be located at the VDD pins of each SO-DIMM connector in the vicinity of the CMD, Clock and Control signals
Those capacitors should be placed on the same side of the motherboard as the SO-DIMM connector

Layout Note:
Place near JDIMM1

Layout Note:
Place near JDIMM1.203,204

JDIMM1
FOX_AS0A626-U2SN-7F
CONN@

M1

M3

M3 Circuit (Processor Generated SO-DIMM VREF_DQ)

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

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Compal Electronics, Inc.

Title: DDRIII DIMMA

Size: | Document Number: LA-8381P | Rev: 1.0

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(8) DDR_B_DQS#[0..7]
(8) DDR_B_DQS[0..7]
(8) DDR_B_D[0..63]
(8) DDR_B_MA[0..15]

All VREF traces should have 10 mil trace width

Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

All VREF traces should have 10 mil trace width

JDIMM2

CONN@

+1.5V_SUS decoupling caps be located at the VDD pins of each SO-DIMM connector in the vicinity of the CMD, Clock and Control signals
Those capacitors should be placed on the same side of the motherboard as the SO-DIMM connector

Layout Note:
Place near JDIMMB

Layout Note:
Place near JDIMMB.203,204

M1
Item3_X02

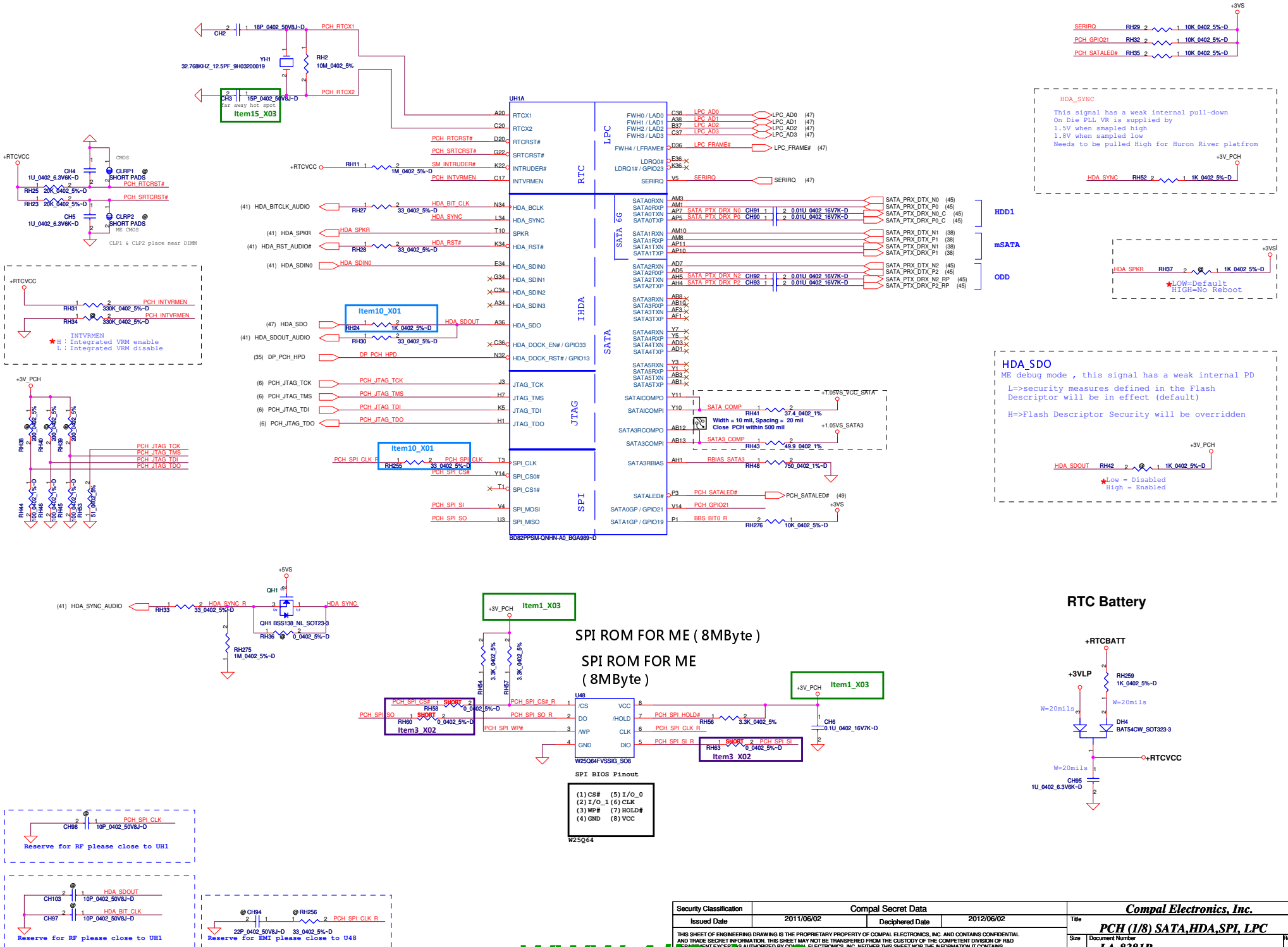
Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: DDRIII DIMMB

Size	Document Number	Rev
	LA-8381P	1.0

Date: Thursday, January 12, 2012 | Sheet 13 of 63



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.			
Title	PCH (1/8) SATA,HDA,SPI, LPC		
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Place TX DC blocking caps close PCH.

10/100/1G LAN --->
MiniDMC (Mini Card 2)--->
MiniWLAN (Mini Card 1)--->
CARD_READER --->

UH1B

PCI-E*

SMBUS

Controller Link

CLOCKS

FLEX CLOCKS

BD82PPSM-QNHN-A0_BGA989-D

Item3_X02

MEMORY

No support iAMT

Item6_X01

Item27_X01

Item3_X02

If use extenal CLK gen, please place close to CLK gen else, please place close to PCH

Reserve for EMI please close to UH1

Reserve for EMI please close to UH1

Width = 10 mil, Spacing = 20 mil
Close PCH within 500 mil

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

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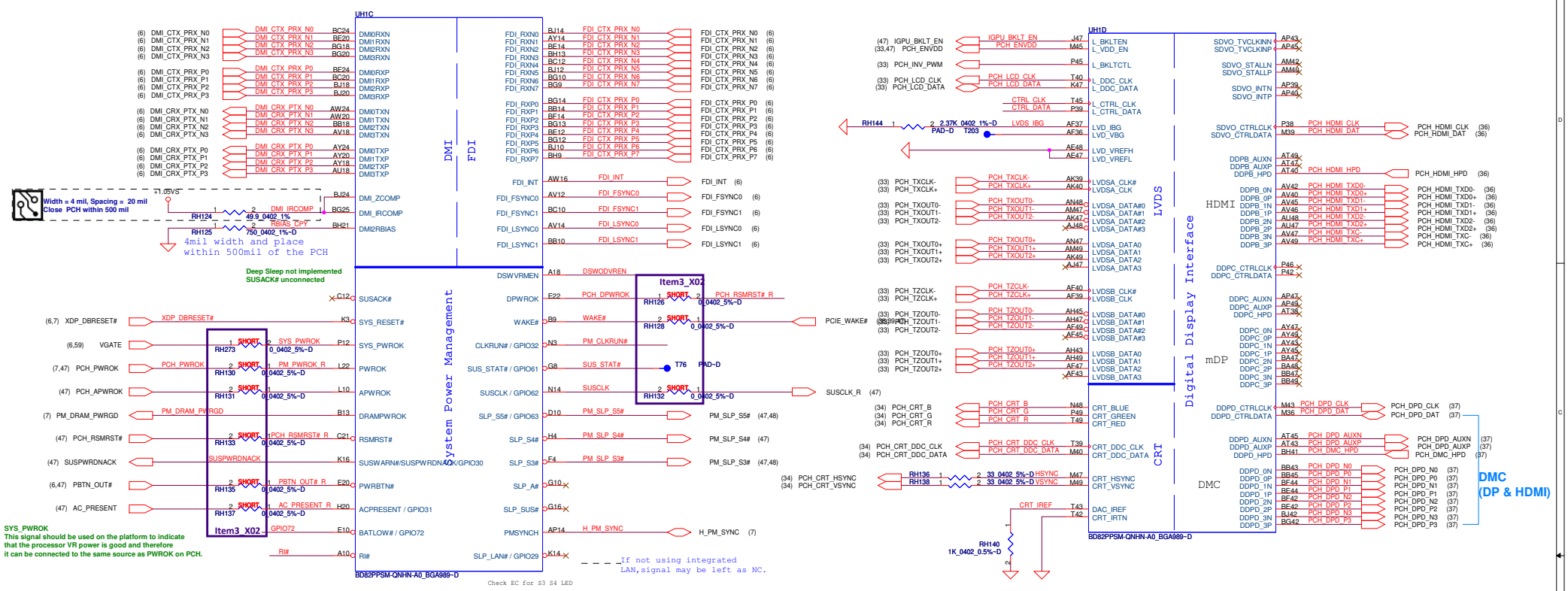
Compal Electronics, Inc.

Title: PCH (2/8) PCIE, SMBUS, CLK

Size	Document Number	Rev
	LA-8381P	1.0

Date: Thursday, January 12, 2012 | Sheet 15 of 63



APWROK
This is a input signal to the PCH from power monitoring circuit to indicate that all Active Sleep Well (ASW) rails, i.e. Intel ME sub-system and LAN power rails are stable on the platform. Connect to ASW power rail monitoring circuit on motherboard. For platform not supporting Intel AMT it can be connected to PWROK. The ASW power must be stable for at least 1ms before platform logic asserts APWROK.

DPWROK
This is an input signal to the PCH from platform power monitoring logic to indicate that all power rails associated with the PCH Deep Sx well (DSW) are valid and stable. Connect to VccDSW3_3 power rail monitoring circuit on mother board for platforms that support Deep Sx state. This signal can be tied to RSMRST# for platforms that do not support the Deep Sx state. The DSW rails must be stable for at least 10ms before DPWROK is asserted to PCH.

CRT_HSYNC and CRT_VSYNC resistor
33 ohm for Direct Connect
20 ohm for Dock Support
20 ohm for Switchable Graphics Device Down Topology
10 ohm for Switchable Graphics Dock Support

Put close PCH 500 mil

Reserve for RF please close to UH1

DSWODVREN - On Die DSW VR Enable
H : Enable
L : Disable

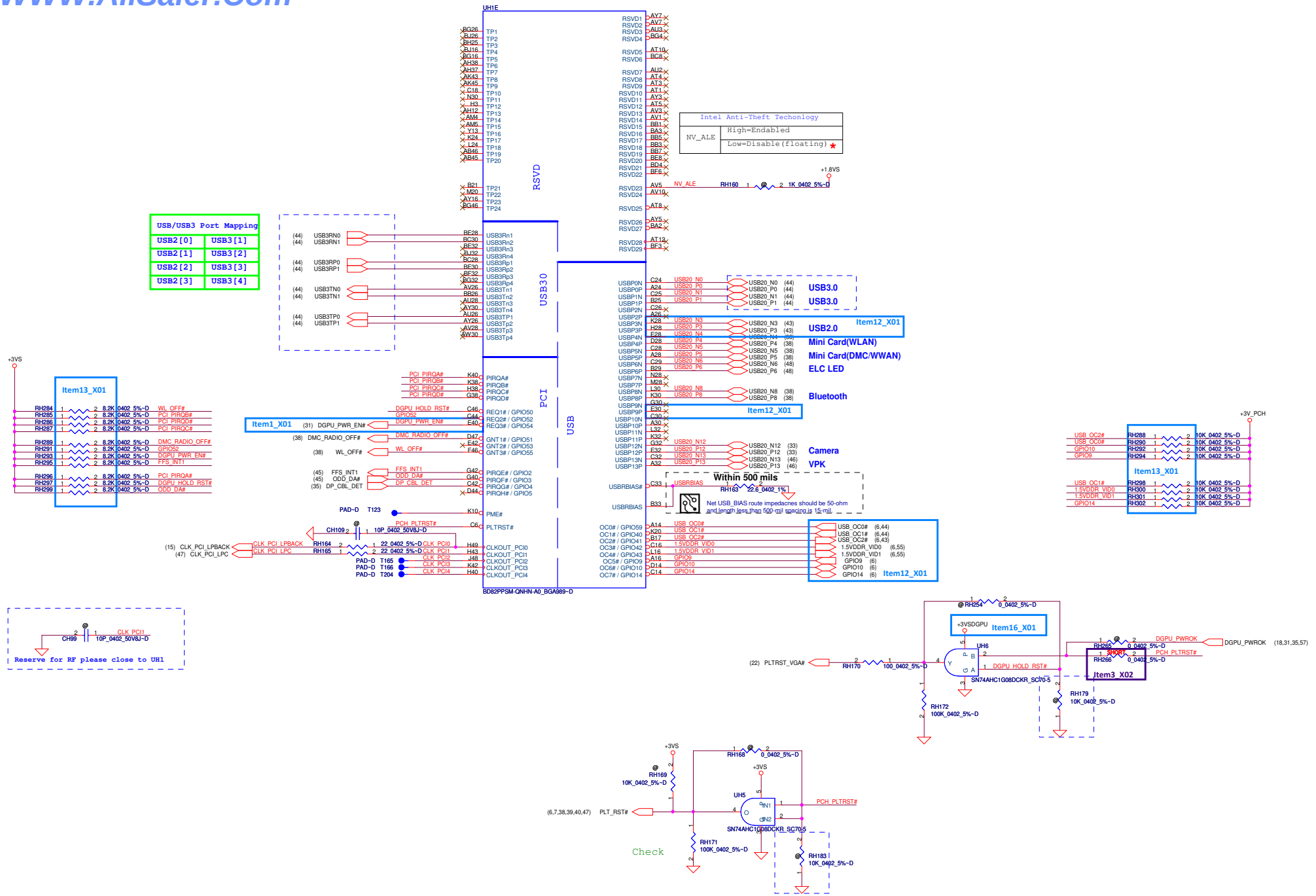
Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: PCH (3/8) DMI,FDI,PM,GFX,DP

Size	Document Number	Rev
	LA-8381P	1.0

Date: Thursday, January 12, 2012 | Sheet 16 of 63



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: PCH (4/8) PCI, USB, NVRAM

Size	Document Number	Rev
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High: CRT Plugged

+3VS
RH198 10K_0402_5%~D
CRT_DET
(34) CRT_DET#
QH5 2N7002K_SOT23-3
Item13_X02

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
★ H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable
+3V_PCH
PCH_GPIO28 RH229 8.2K_0402_5%~D
RH177 1K_0402_5%~D PCH_GPIO28

PCH_GPIO37
FDI TERMINATION VOLTAGE OVERRIDE
★ LOW - Tx, Rx terminated to same voltage (DC Coupling Mode)
+3VS
RH181 1K_0402_5%~D PCH_GPIO37
RH182 10K_0402_5%~D PCH_GPIO37

UH1F

	CRT_DET	T7	BMBUSY# / GPIO0		
		A42	TACH1 / GPIO1		
	GPIO6	H36	TACH2 / GPIO6		
(47)	EC_SCI#	E38	TACH3 / GPIO7		
(47)	EC_SMI#	C10	GPIO8		
(38)	BT_RADIO_DIS#	C4	LAN_PHY_PWR_CTRL / GPIO12		
(6)	GPIO15	G2	GPIO15		
	GPIO16	U2	SATA4GP / GPIO16		
(17,31,35,57)	DGPU_PWROK	D40	TACH0 / GPIO17		
	PCH_GPIO22	T5	SCLOCK / GPIO22		
		E8	GPIO24		
		E16	GPIO27		
	PCH_GPIO28	P8	GPIO28		
(38)	BT_ON#	K1	STP_PCI# / GPIO34		
	GPIO35	K4	GPIO35		
(45)	ODD_DETECT#	V8	SATA2GP / GPIO36		
	PCH_GPIO37	M5	SATA3GP / GPIO37		
	DGPU_PRSNT#	N2	SLOAD / GPIO38		
	PCH_GPIO39	M3	SDATAOUT0 / GPIO39		
(45)	FFS_INT2	V13	SDATAOUT1 / GPIO48		
	GPIO49	V3	SATA5GP / GPIO49 / TEMP_ALERT#		
(45)	HDD_DETECT#	D6	GPIO57		
		A4	VSS_NCTF_1		
		A44	VSS_NCTF_2		
		A45	VSS_NCTF_3		
		A46	VSS_NCTF_4		
		A5	VSS_NCTF_5		
		A6	VSS_NCTF_6		
		B3	VSS_NCTF_7		
		B47	VSS_NCTF_8		
		BD1	VSS_NCTF_9		
		BD49	VSS_NCTF_10		
		BE1	VSS_NCTF_11		
		BE49	VSS_NCTF_12		
		BF1	VSS_NCTF_13		
		BF49	VSS_NCTF_14		
				TACH4 / GPIO68	C40 ODD_EN# (45)
				TACH5 / GPIO69	B41 GPIO69 T126 PAD~D
				TACH6 / GPIO70	C41
				TACH7 / GPIO71	A40
				A20GATE	P4 GATEA20 GATEA20 (47)
				PECI	AU16 PCH_PECI_R 0_0402_5%~D H_PECI (7,47)
				RCIN#	P5 KB_RST# KB_RST# (47)
				PROCPWRGD	AY11 H_CPUPWRGD (6,7)
				THRMTRIP#	AY10 H_THERMTRIP# 390_0402_5% H_THERMTRIP# (7)
				INIT3_3V#	T14 INIT3_3V# T127 PAD~D
				DF_TVS	AY1 NV_CLE
				TS_VSS1	AH8
				TS_VSS2	AK11
				TS_VSS3	AH10
				TS_VSS4	AK10
				NC_1	P37
				VSS_NCTF_15	BG2
				VSS_NCTF_16	BG48
				VSS_NCTF_17	BH3
				VSS_NCTF_18	BH47
				VSS_NCTF_19	BJ4
				VSS_NCTF_20	BJ44
				VSS_NCTF_21	BJ45
				VSS_NCTF_22	BJ46
				VSS_NCTF_23	BJ5
				VSS_NCTF_24	BJ6
				VSS_NCTF_25	C2
				VSS_NCTF_26	C48
				VSS_NCTF_27	D1
				VSS_NCTF_28	D49
				VSS_NCTF_29	E1
				VSS_NCTF_30	E49
				VSS_NCTF_31	F1
				VSS_NCTF_32	F49

GPIO
CPU/MISC
NCTF
BD82PPSM-QNHN-A0_BGA989~D

INIT3_3V
This signal has weak internal PU, can't pull low

DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH
	Set to Vss when LOW

+1.8VS
Weak internal PU,Do not pull low
RH161 2.2K_0402_5%~D
NV_CLE 1K_0402_5%~D RH162 H_SNB_IVB# (7)
CLOSE TO THE BRANCHING POINT
RH161 and RH162 Follow CRB FAB2 setting

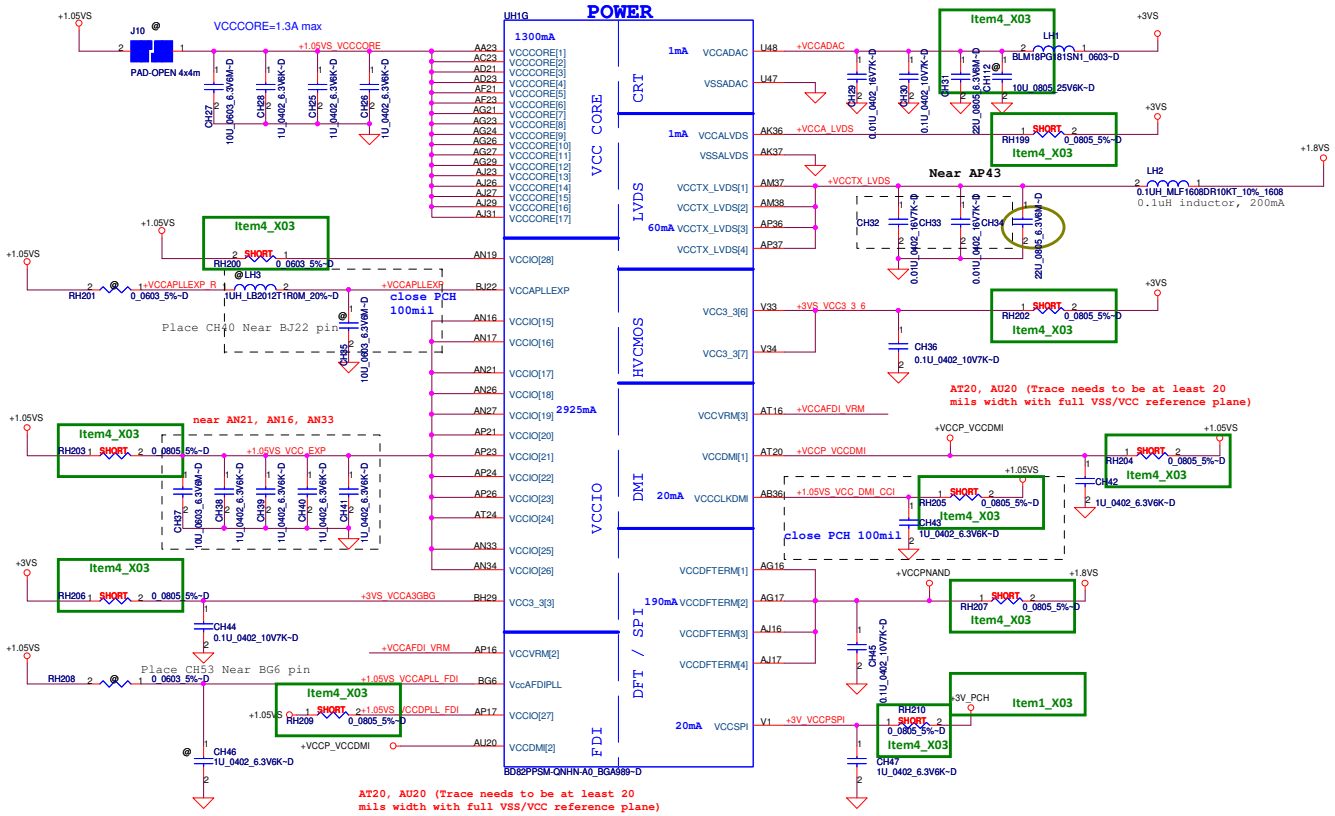
+3V_PCH
HDD_DETECT# RH188 10K_0402_5%~D
EC_SMI# RH190 10K_0402_5%~D
BT_RADIO_DIS# RH279 10K_0402_5%~D
GPIO15 RH281 1K_0402_5%~D

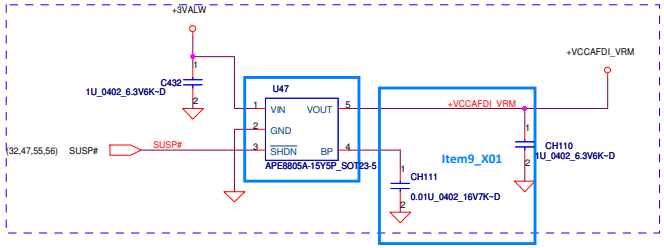
+3VS
ODD_EN# RH187 10K_0402_5%~D
CRT_DET# RH192 10K_0402_5%~D
ODD_DETECT# RH193 200K_0402_5%
GPIO16 RH274 10K_0402_5%~D
BT_ON# RH195 8.2K_0402_5%~D
KB_RST# RH196 10K_0402_5%~D
PCH_GPIO22 RH197 10K_0402_5%~D
GPIO35 RH257 10K_0402_5%~D
GPIO49 RH258 10K_0402_5%~D
PCH_GPIO39 RH263 10K_0402_5%~D
GPIO6 RH271 10K_0402_5%~D
GATEA20 RH174 10K_0402_5%~D
EC_SCI# RH283 10K_0402_5%~D

For BIOS setting dGPU present
★ LOW - dGPU exist
+3VS
DGPU_PRSNT# RH262 10K_0402_5%~D
DGPU_PRSNT# RH282 10K_0402_5%~D

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.
Title: PCH (5/8) GPIO, CPU, MISC
Size: | Document Number: LA-8381P | Rev: 1.0
Date: Thursday, January 12, 2012 | Sheet 18 of 63





PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

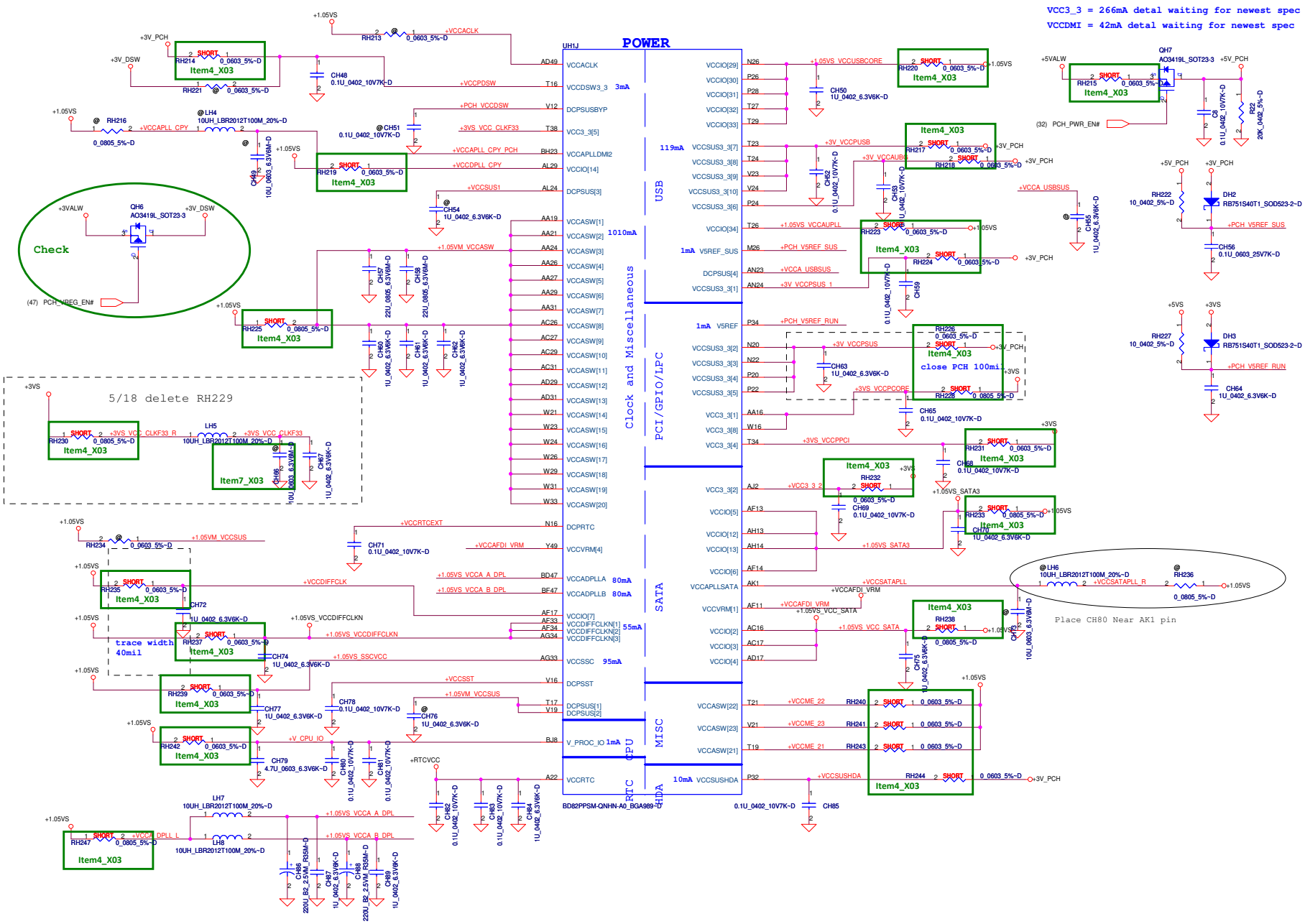
Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: PCH (6/8) PWR

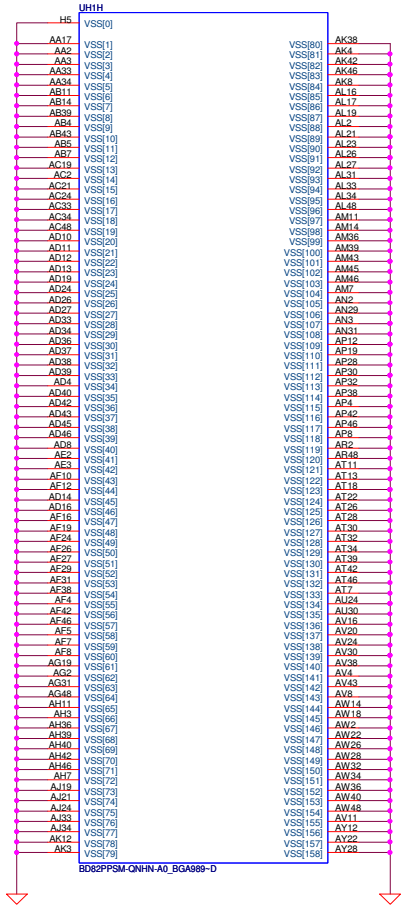
Size: | Document Number: LA-8381P | Rev: 1.0

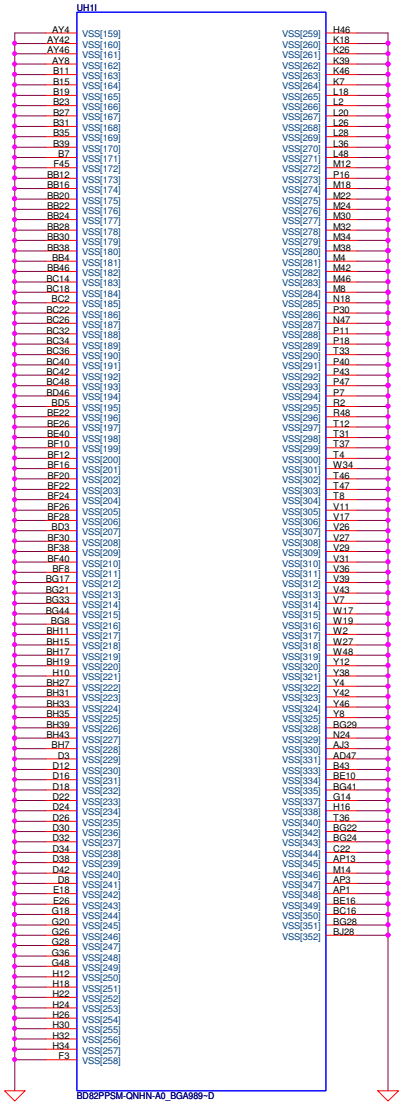
Date: Thursday, January 12, 2012 | Sheet 19 of 63



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.			
Title	PCH (7/8) PWR		
Size	Document Number		Rev
	LA-8381P		1.0
Date:	Thursday, January 12, 2012	Sheet	20 of 63





Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.			
Title: PCH (8/8) VSS			
Size	Document Number: LA-8381P		Rev: 1.0
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GPIO	I/O	USAGE
GPIO0	O	GPU_VID4
GPIO1	O	GPU_VID3
GPIO2	O	NC
GPIO3	O	DPRSLPVR (reserve)
GPIO4	O	NC
GPIO5	O	GPU_VID1
GPIO6	O	GPU_VID2
GPIO7	O	NC
GPIO8	I/O	OVERT (10K pull High)
GPIO9	I/O	ALERT (10K pull High)
GPIO10	O	MEM_VREF_CTL
GPIO11	O	GPU_VID0
GPIO12	I	GPU_DC# (10K pull High)
GPIO13	O	GPU_VID5
GPIO14	I	NC
GPIO15	I	NC
GPIO16	O	DPRSLPVR (reserve)
GPIO17	I	VGA_mDP_HPD
GPIO18	I	NC
GPIO19	I	NC
GPIO20		Reserved
GPIO21		Reserved

DACA_VDD 10K pull down,
DACA_VREF, DACA_REST NC

under GPU close to ball : AD8

under GPU close to ball : AE8,AD7

04/06 : Add 6bit VID Function.

N13P-GT boot voltage: confirm Nvidia

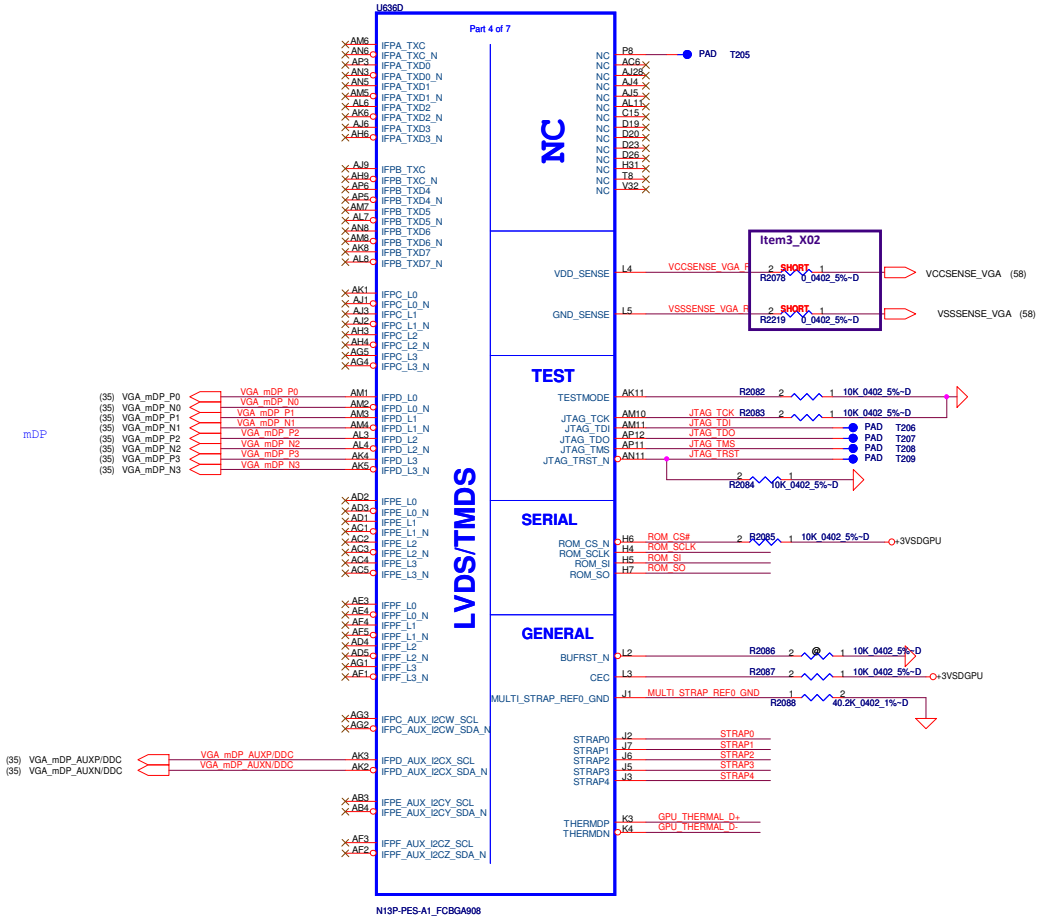
Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: N13P (1/10) PEG,DAC

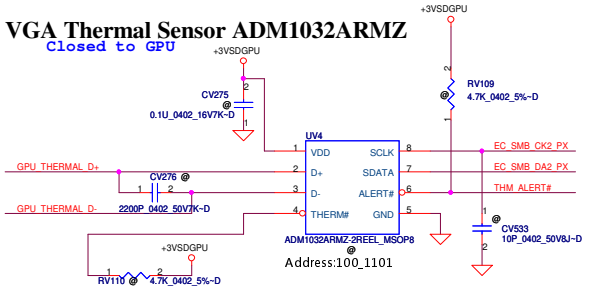
Size	Document Number	Rev
C	LA-8381P	0.1

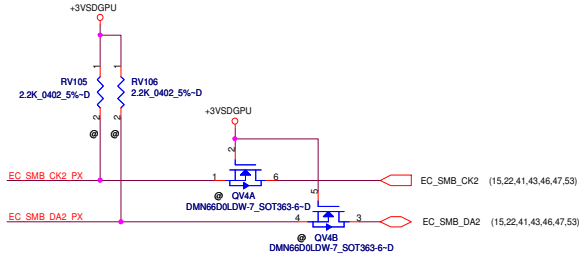
Date: Thursday, January 12, 2012 Sheet 22 of 63



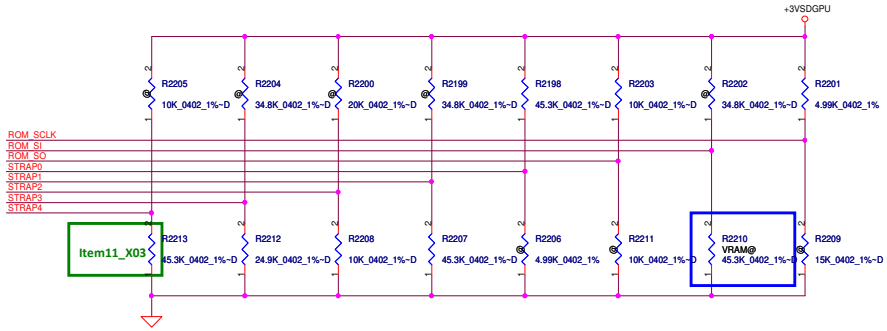
VGA Thermal Sensor ADM1032ARMZ

Closed to GPU





MULTI LEVEL STRAPS



For N13P-GT strap table

GPU	Frenq.	Memory Size	Memory Config	ROM_SCLK	ROM_SI	ROM_SO	STRAP0	STRAP1 (PCIe driving)	STRAP2 (ES PH20K)	STRAP3	STRAP4
N13P-GT	2500 MHz	64M* 16* 8 1GB	Samsung SA00003RS0L	PH 5K	PL 45.3K SD03445328L	PH 10K	PH 45K	PL 45K	PL 10K	PL 25K	PL 10K
N13P-GT	2500 MHz	64M* 16* 8 1GB	Hynix SA00003WL0L	PH 5K	PL 34.8K SD03434828L	PH 10K	PH 45K	PL 45K	PL 10K	PL 25K	PL 10K
N13P-GT	2500 MHz	128M* 16* 8 2GB	Samsung SA000048E0L	PH 5K	PL 30.1K SD03430128L	PH 10K	PH 45K	PL 45K	PL 10K	PL 25K	PL 10K
N13P-GT	2500 MHz	128M* 16* 8 2GB	Hynix SA00004GD0L	PH 5K	PL 24.9K SD03424928L	PH 10K	PH 45K	PL 45K	PL 10K	PL 25K	PL 10K

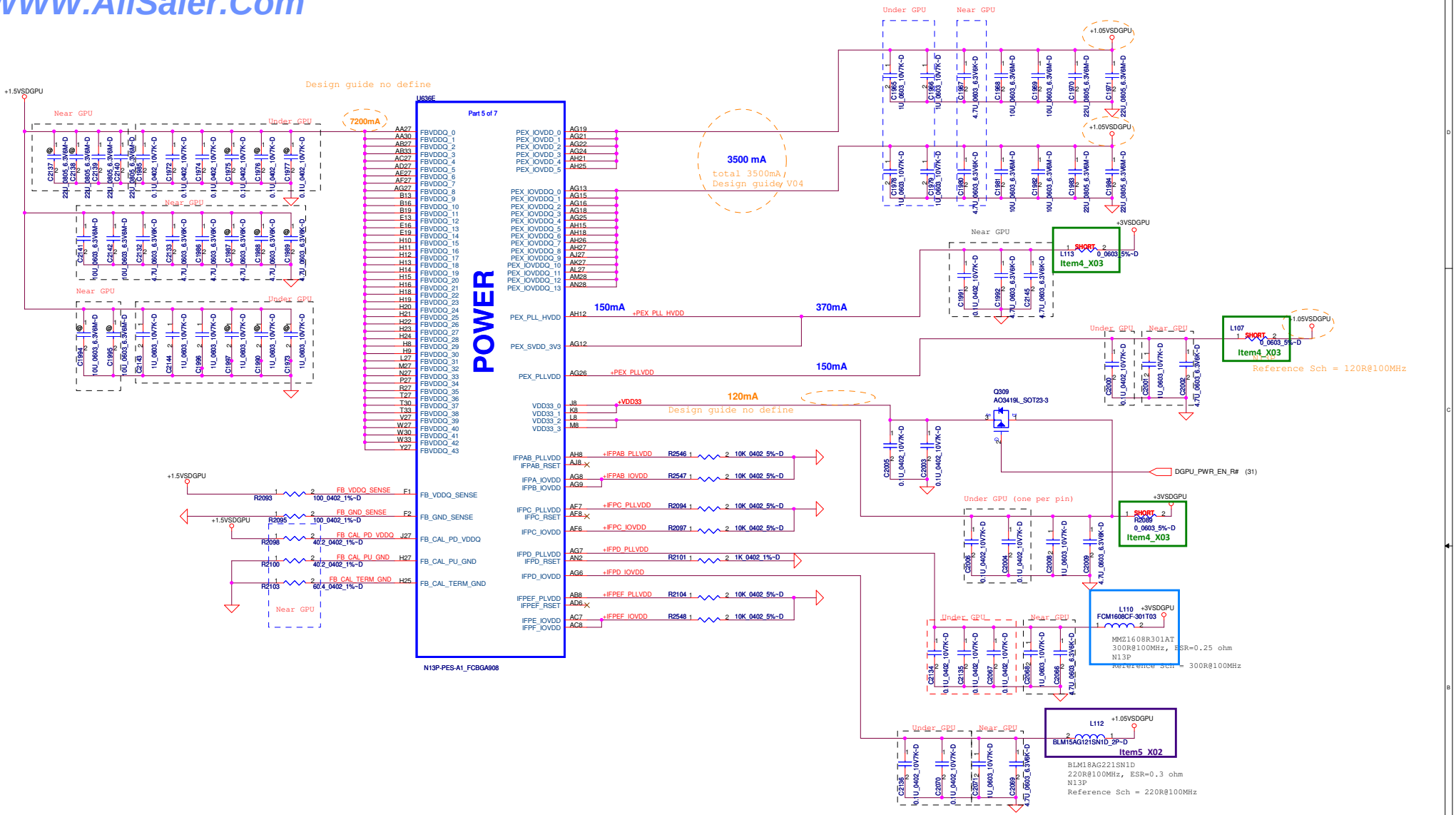
Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: N13P (2/10) mDP, Strapping

Size	Document Number	Rev
C	LA-8381P	0.1

Date: Thursday, January 12, 2012 | Sheet 23 of 63



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.			
Title	N13P (3/10) POWER & GND		
Size	Document Number		Rev
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U636F

Part 6 of 7

GND

N13P-PES-A1_FCBGA908

U636G

Part 7 of 7

POWER

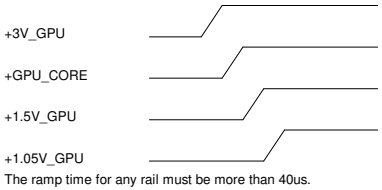
+VGA_CORE

+VGA_CORE

N13P-PES-A1_FCBGA908

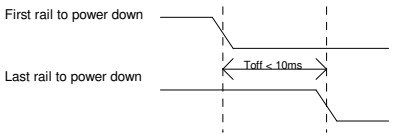
SEQUENCE

GPU Power Up Power Rail Sequence

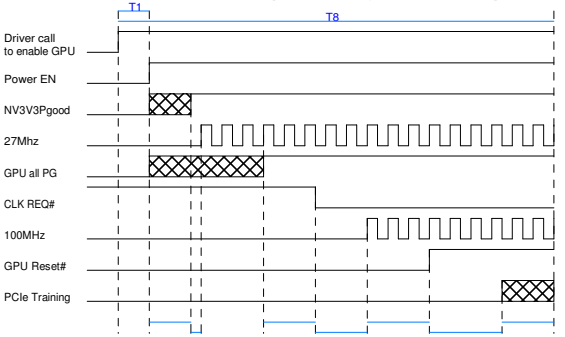


The ramp time for any rail must be more than 40us.

GPU Power Down Sequence



GPU Power Up Sub-system Sequence



GPU Power Up Sub-system Sequence

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: N13P (4/10) POWER & GND

Size	Document Number	Rev
C	LA-8381P	0.1

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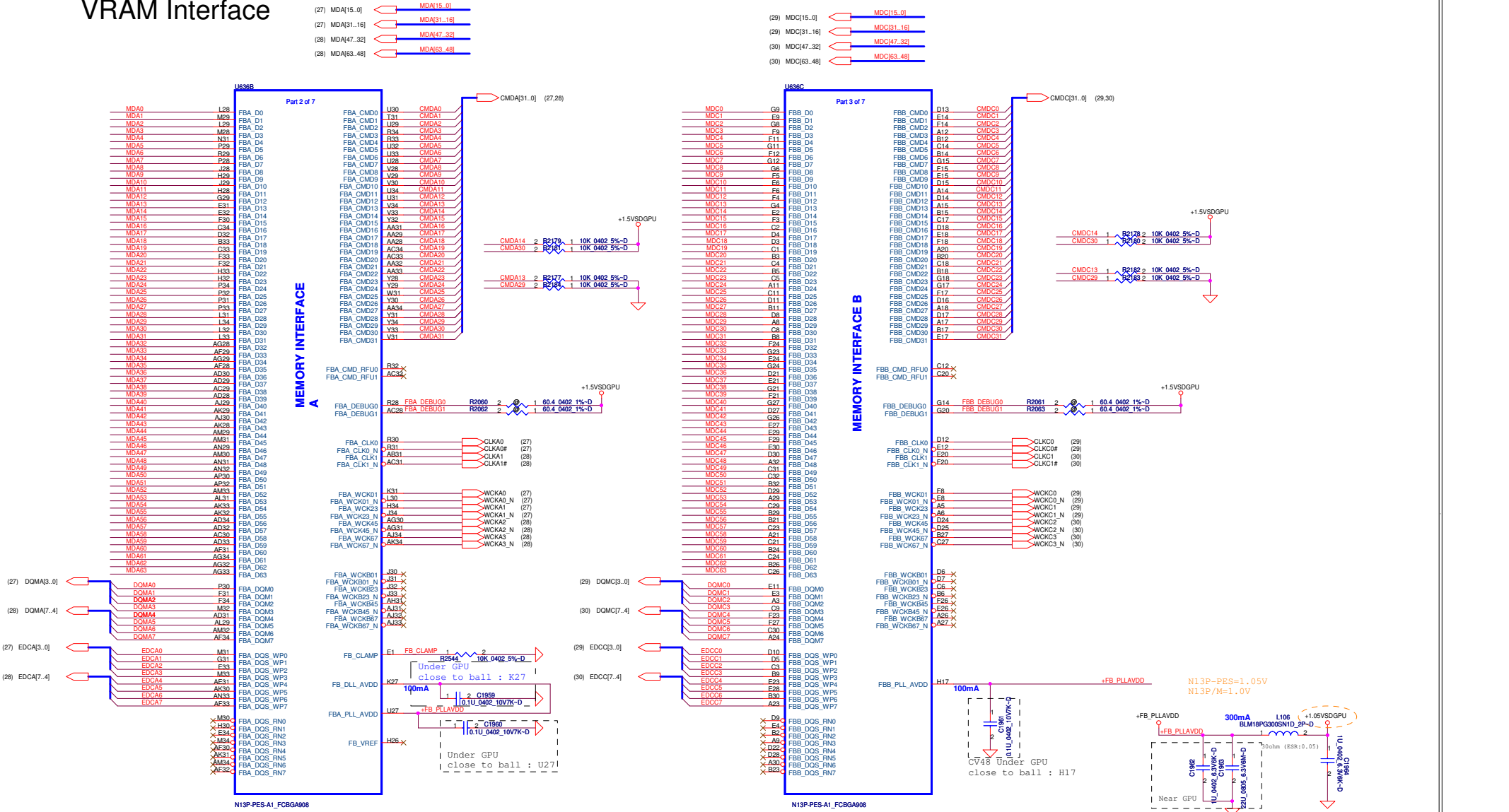
VRAM Interface



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

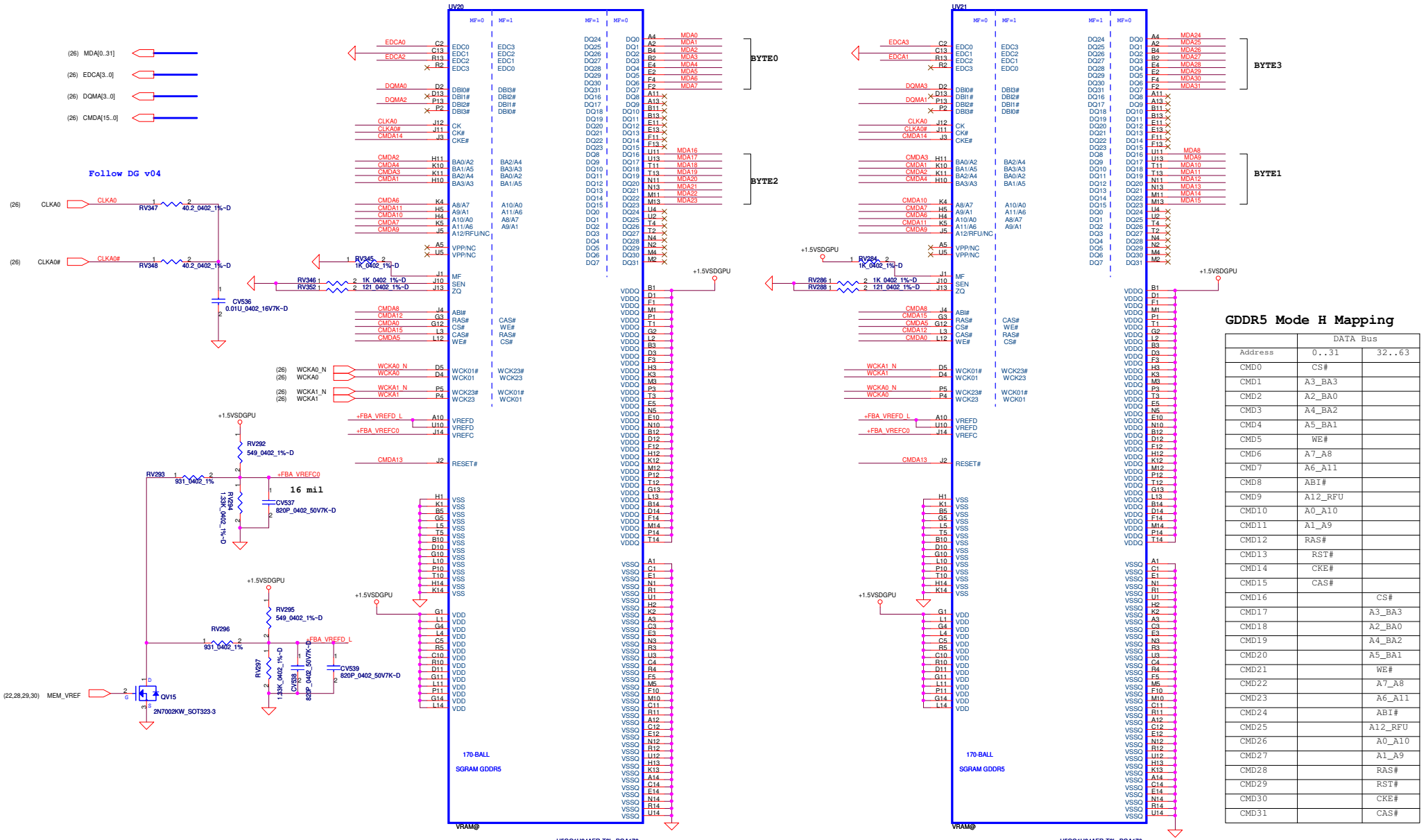
Compal Electronics, Inc.

Title: N13P (5/10) VRAM interface

Size	Document Number	Rev
C	LA-8381P	0.1

Date: Thursday, January 12, 2012 Sheet 26 of 63

Memory Partition A - Lower 32 bits



GDDR5 Mode H Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI#
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#

Compal Electronics, Inc.
Title: N13P (6/10) VRAM A Lower
Size | Document Number: LA-8381P | Rev: 0.3
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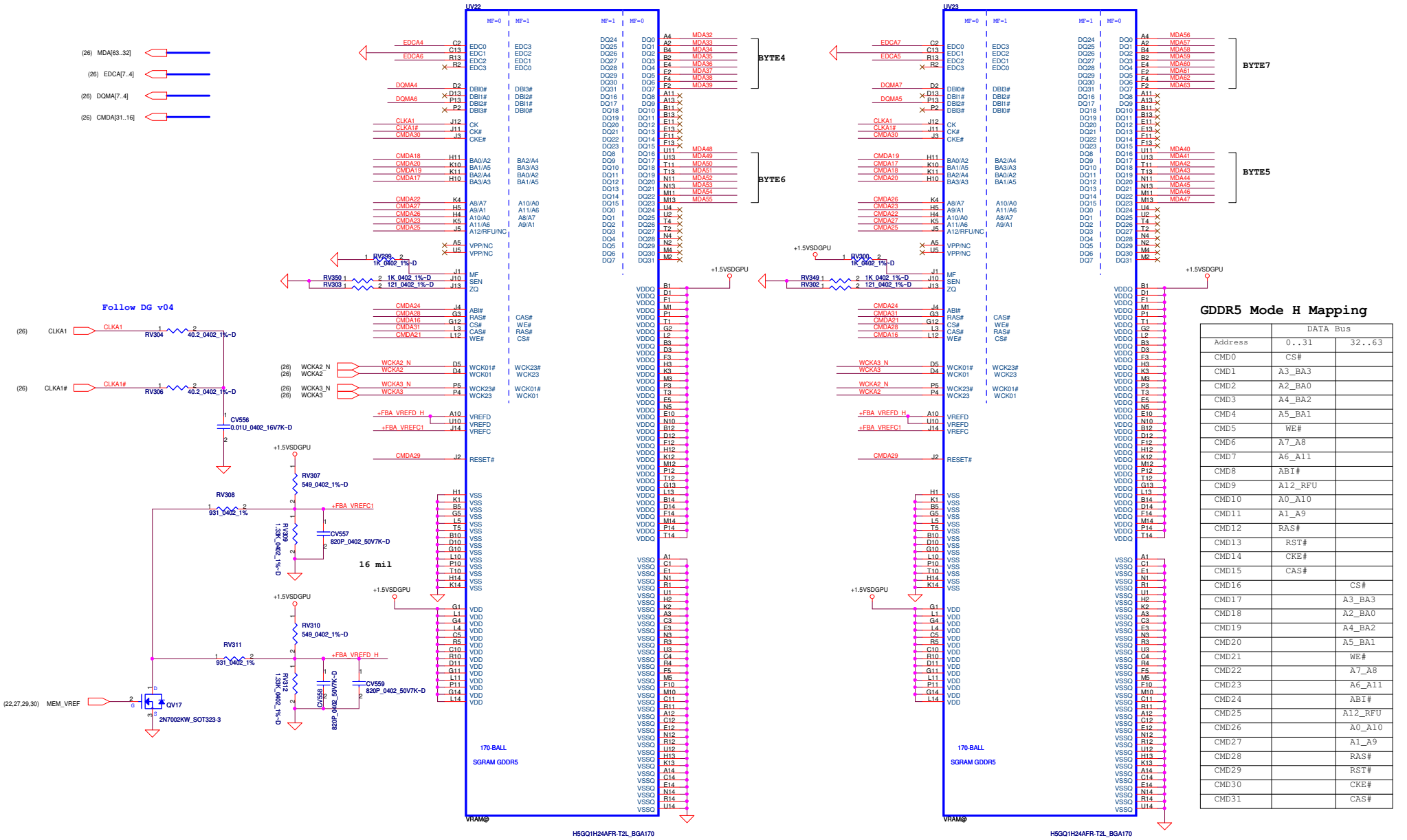
Memory Partition A - Upper 32 bits



GDDR5 Mode H Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI#
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: N13P (7/10) VRAM A Upper

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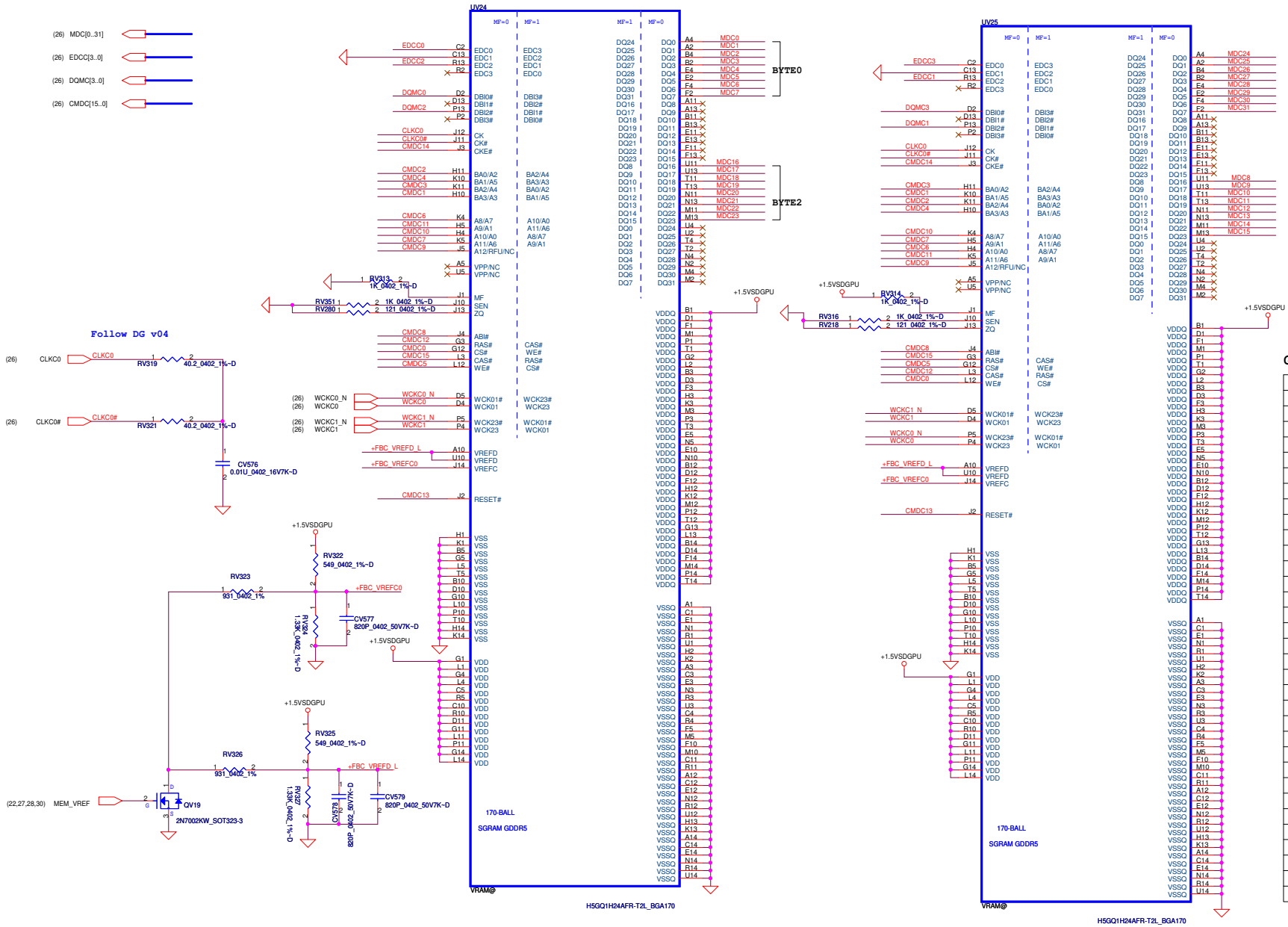
Memory Partition C - Lower 32 bits



GDDR5 Mode H Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI#
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#

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Title	N13P (8/10) VRAM B Lower		
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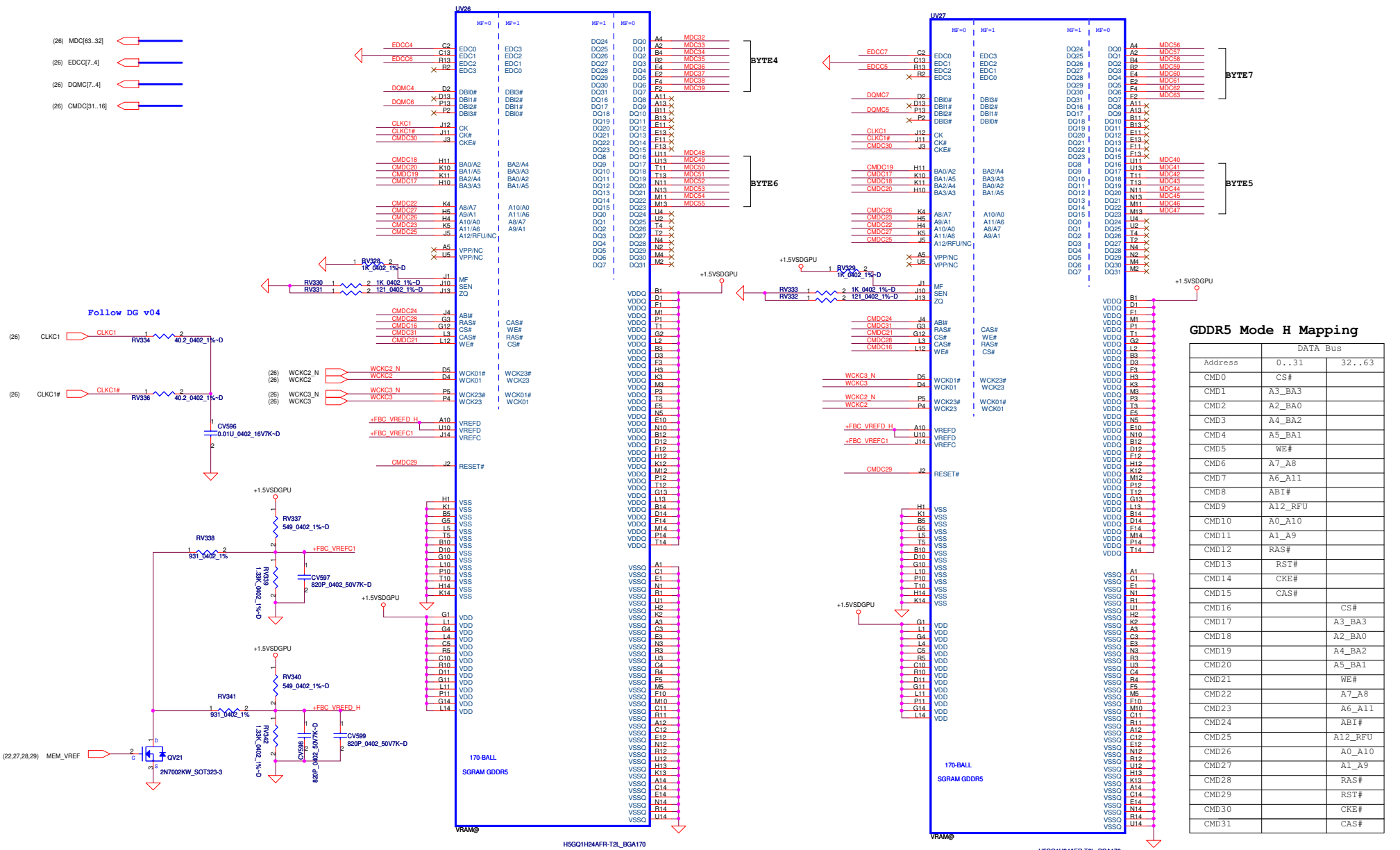
Memory Partition C -- Upper 32 bits



GDDR5 Mode H Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI#
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: N13P (9/10) VRAM B Upper

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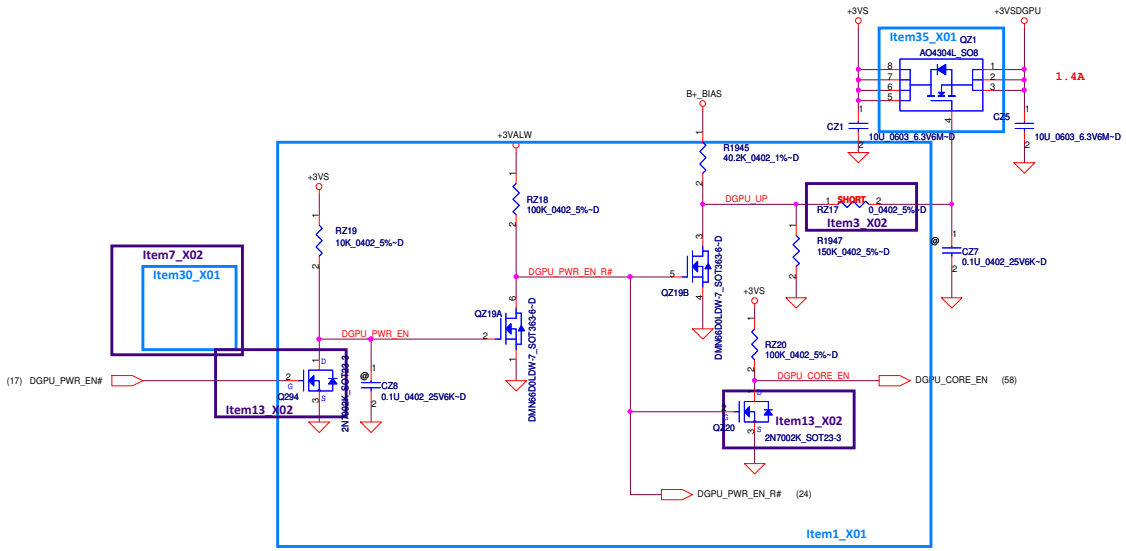
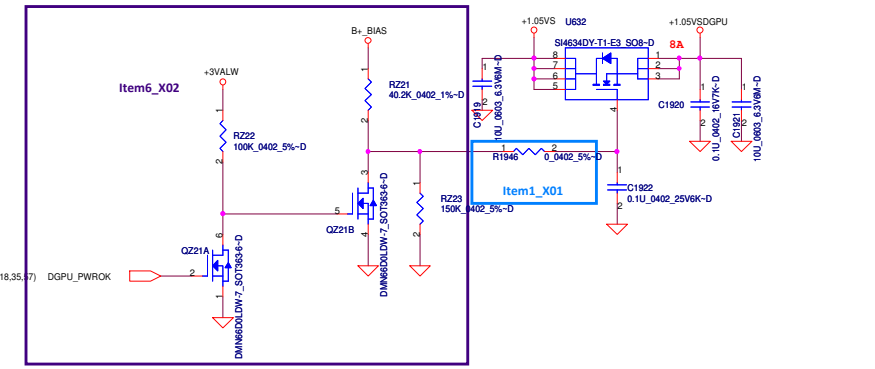
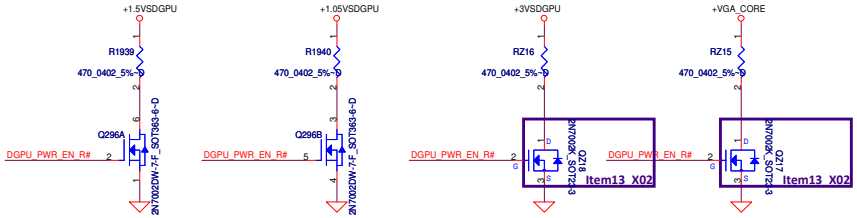
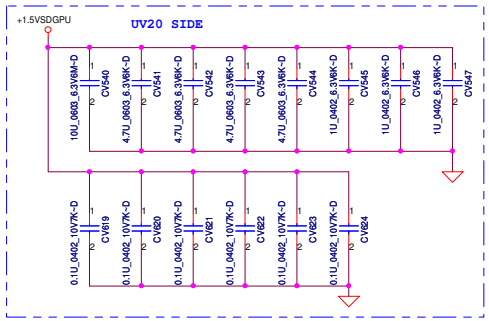
+3VS to +3VSDGPU

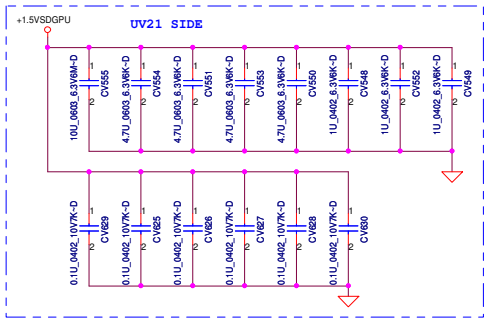
+1.05V to +1.05VSDGPU Transfer

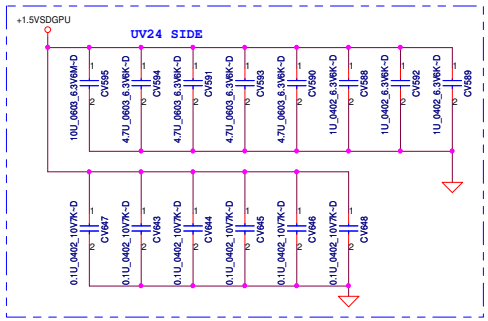


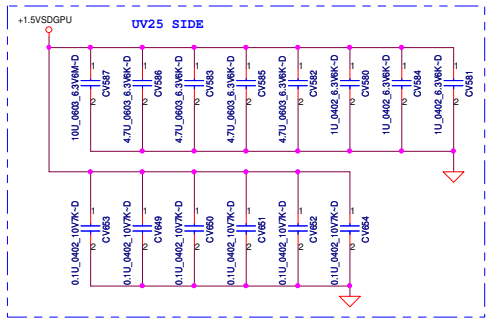


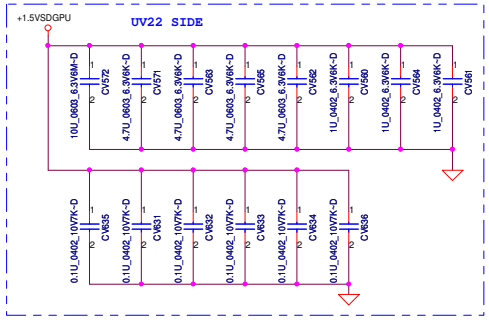


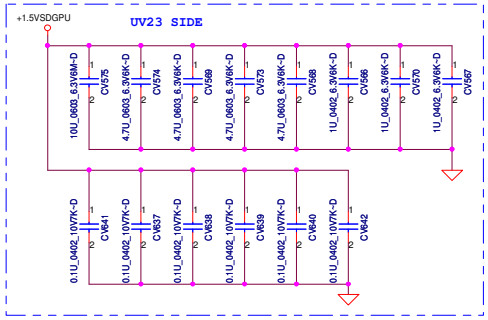


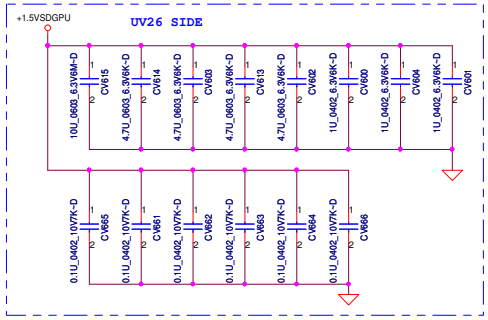


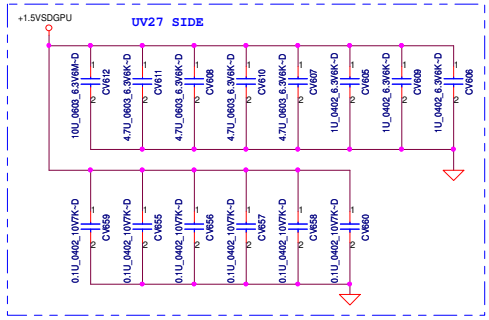












Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: N13P (10/10) DC/DC interface

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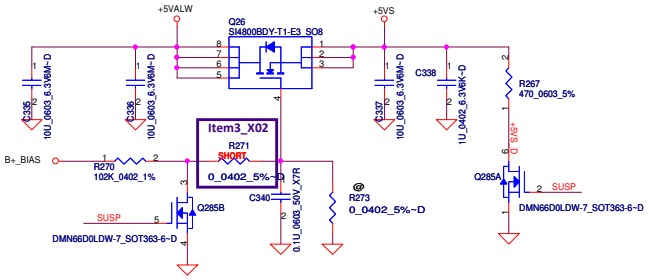
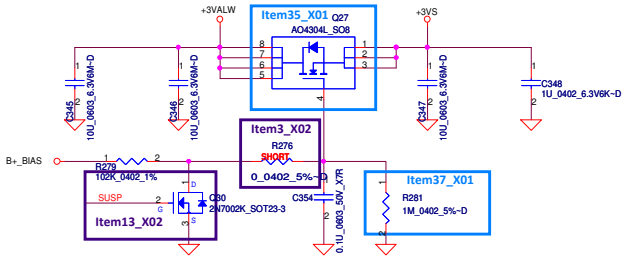
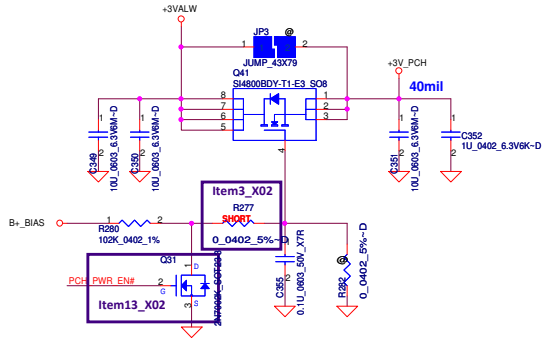
+5VALW to +5VS



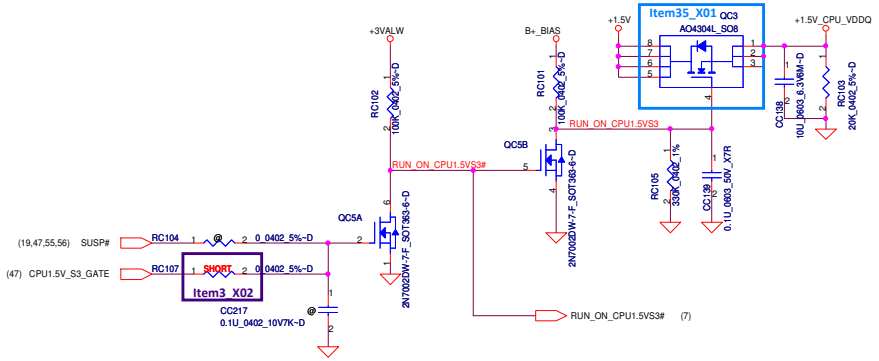
+3VALW to +3VS

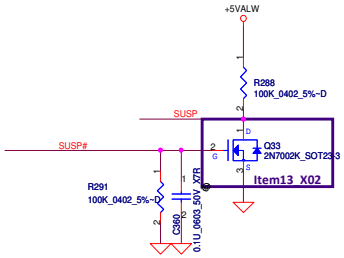


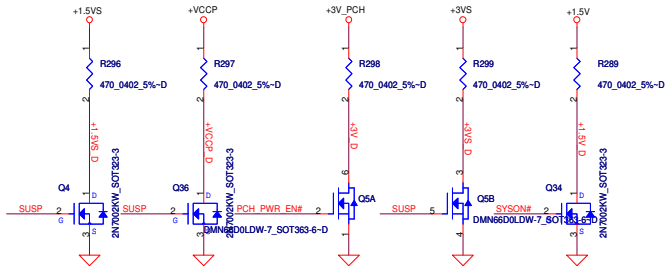
+3VALW to +3V_PCH

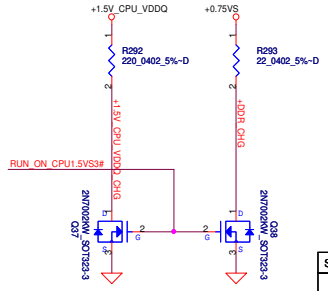


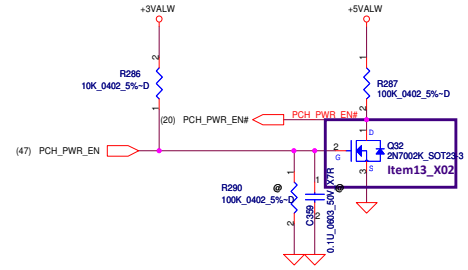
+1.5V to +1.5V_CPU_VDDQ

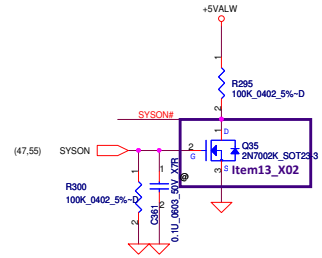












Compal Electronics, Inc.

Title: DC/DC Interface

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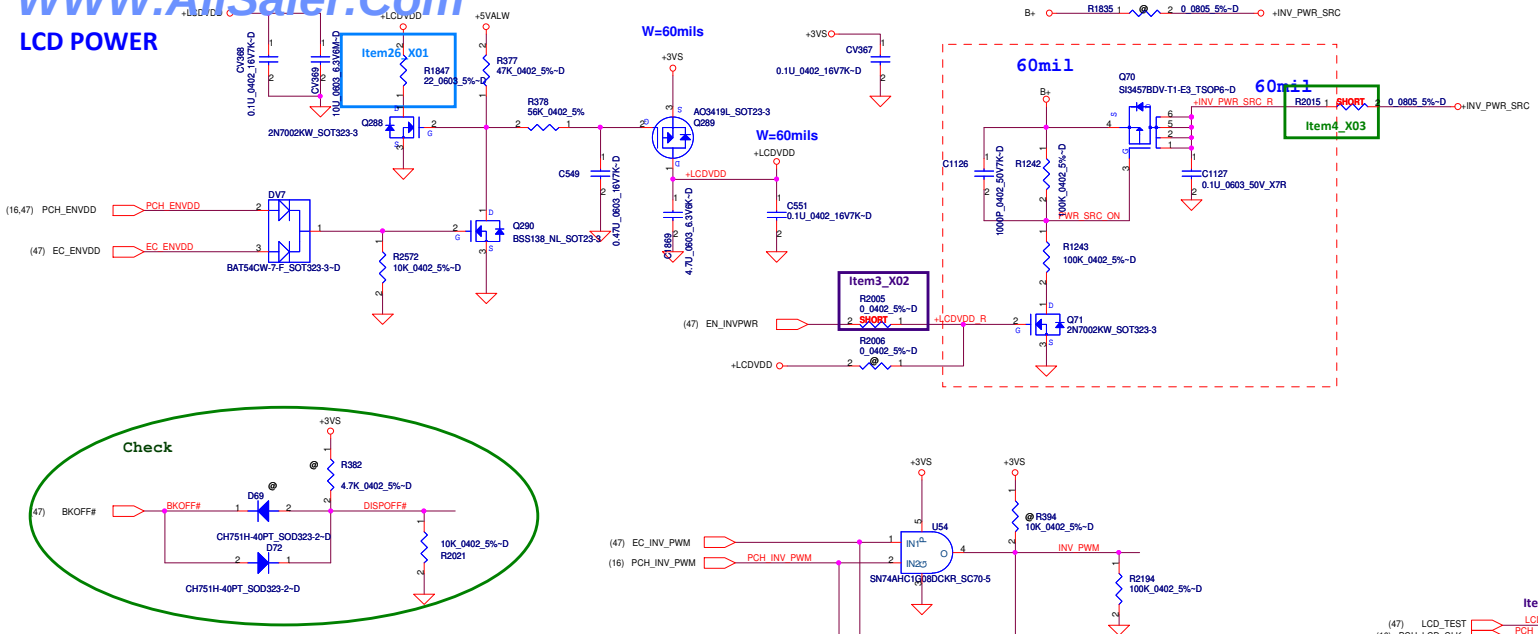
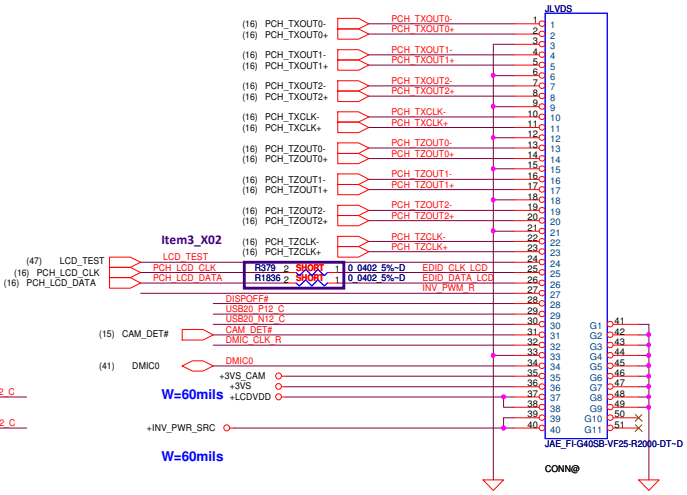
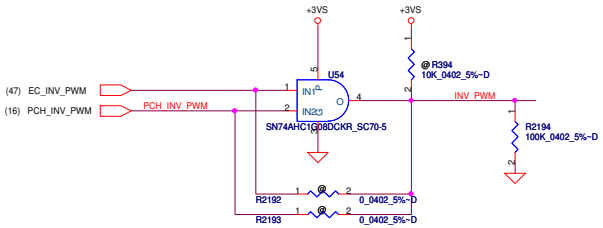
LCD POWER

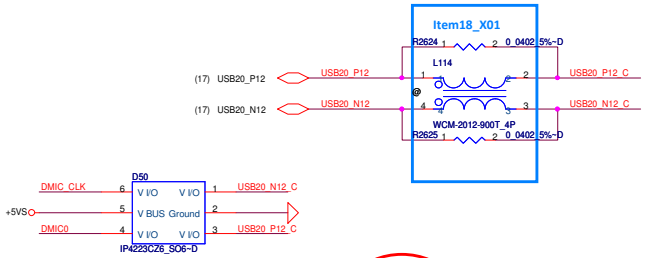


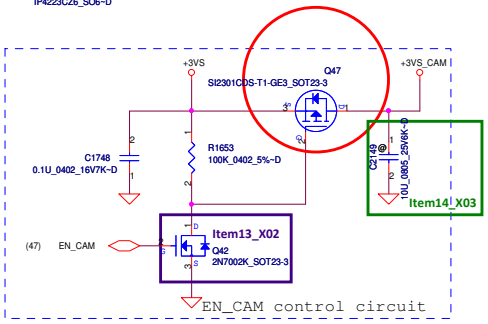
LVDS Conn.

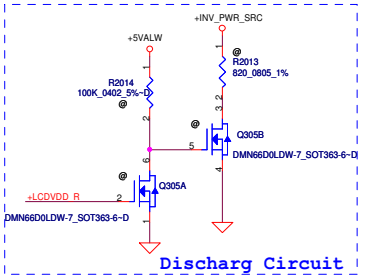


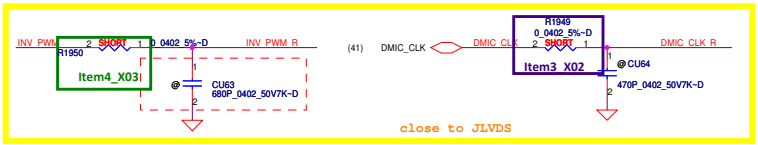


LCD Backlight Selector









Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: LVDS SW-6038 /camera conn.

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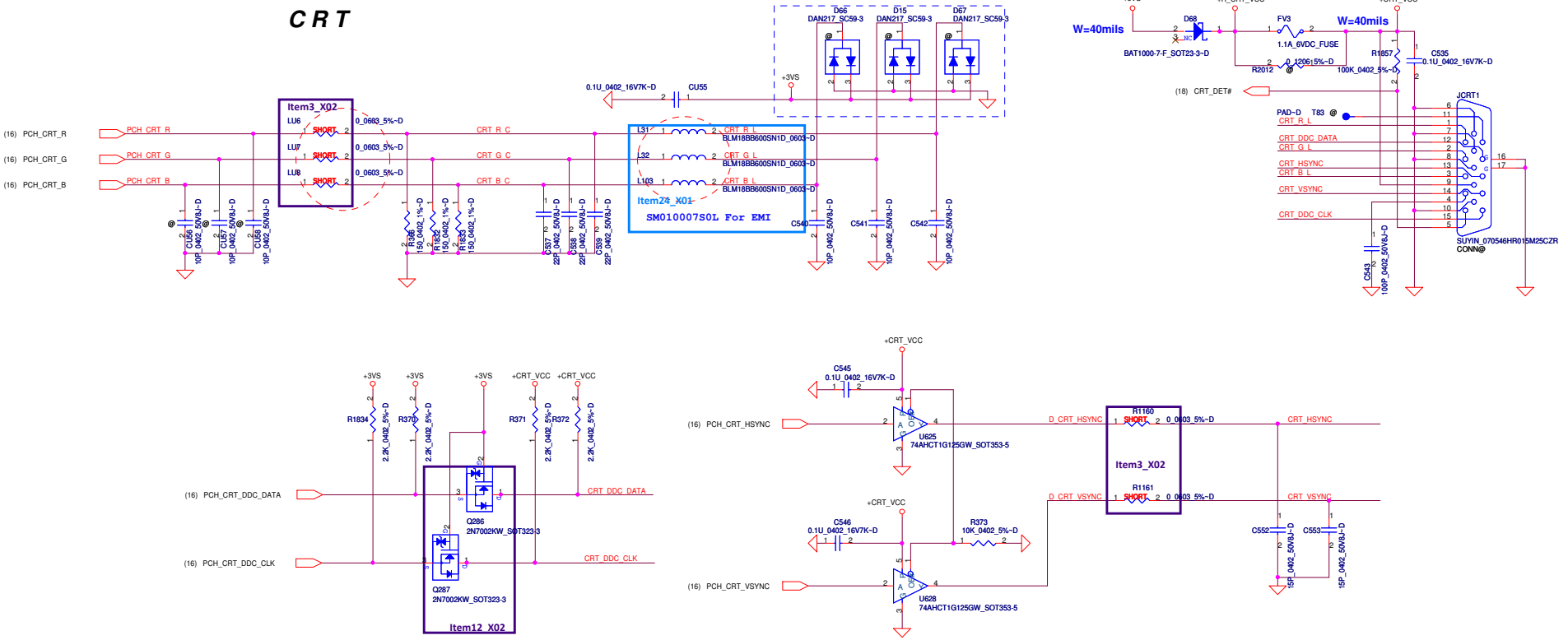
CRT



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.			
Title: VGA Conn.			
Size	Document Number: LA-8381P		Rev: 1.0
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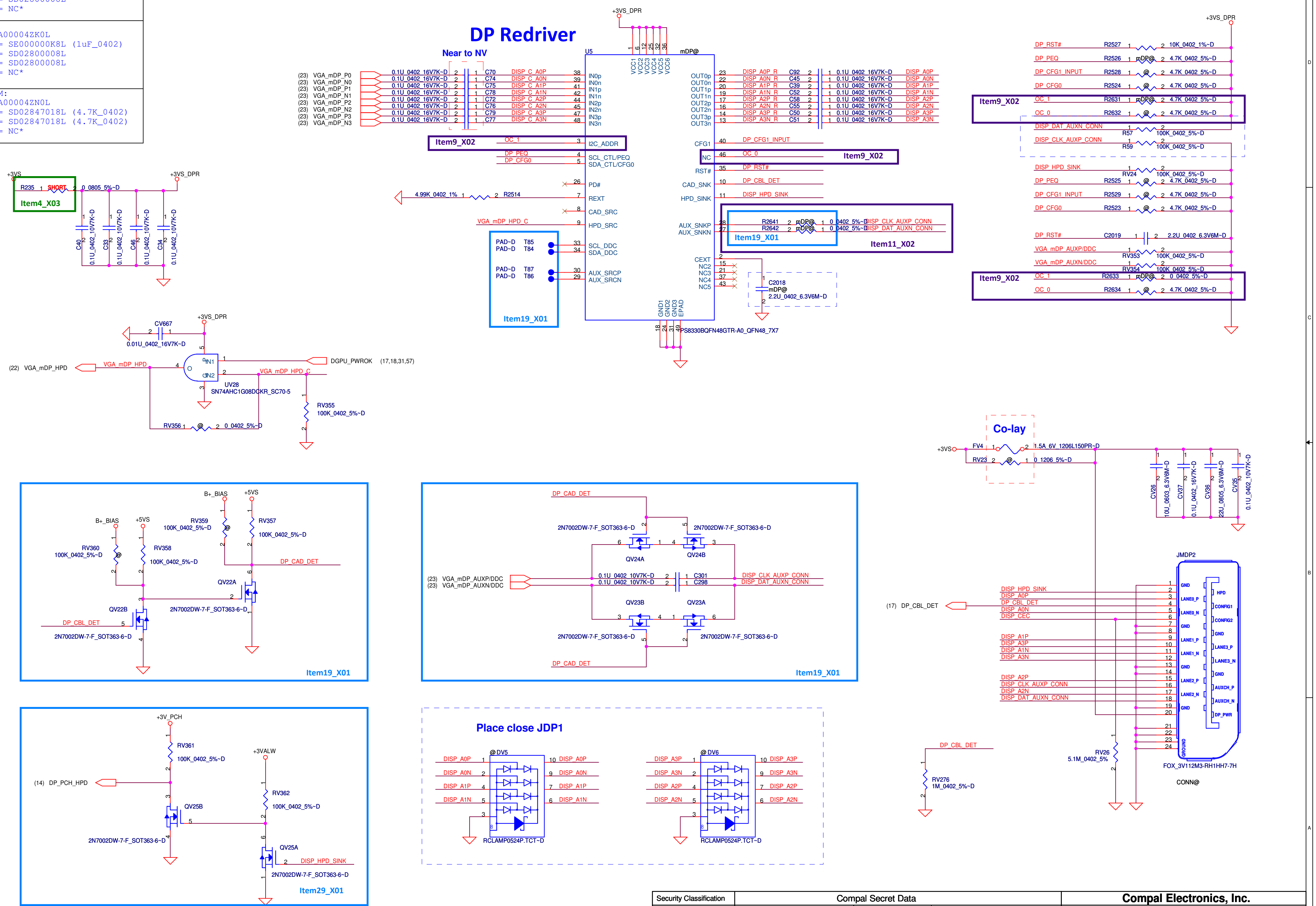
X76 BOM option table

PARADE:
U5 = SA00004ZM00
C2018 = SE00000888L (2.2uF_0402)
R2633 = SD02800008L
Other = NC*

TI:
U5 = SA00004ZK0L
C2018 = SE000000K8L (1uF_0402)
R2641 = SD02800008L
R2642 = SD02800008L
Other = NC*

PERICOM:
U5 = SA00004ZN0L
R2526 = SD02847018L (4.7K_0402)
R2631 = SD02847018L (4.7K_0402)
Other = NC*



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Issued Date	2011/06/02	Deciphered Date	2012/06/02

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Compal Electronics, Inc.

Title: **Mini Display Port**

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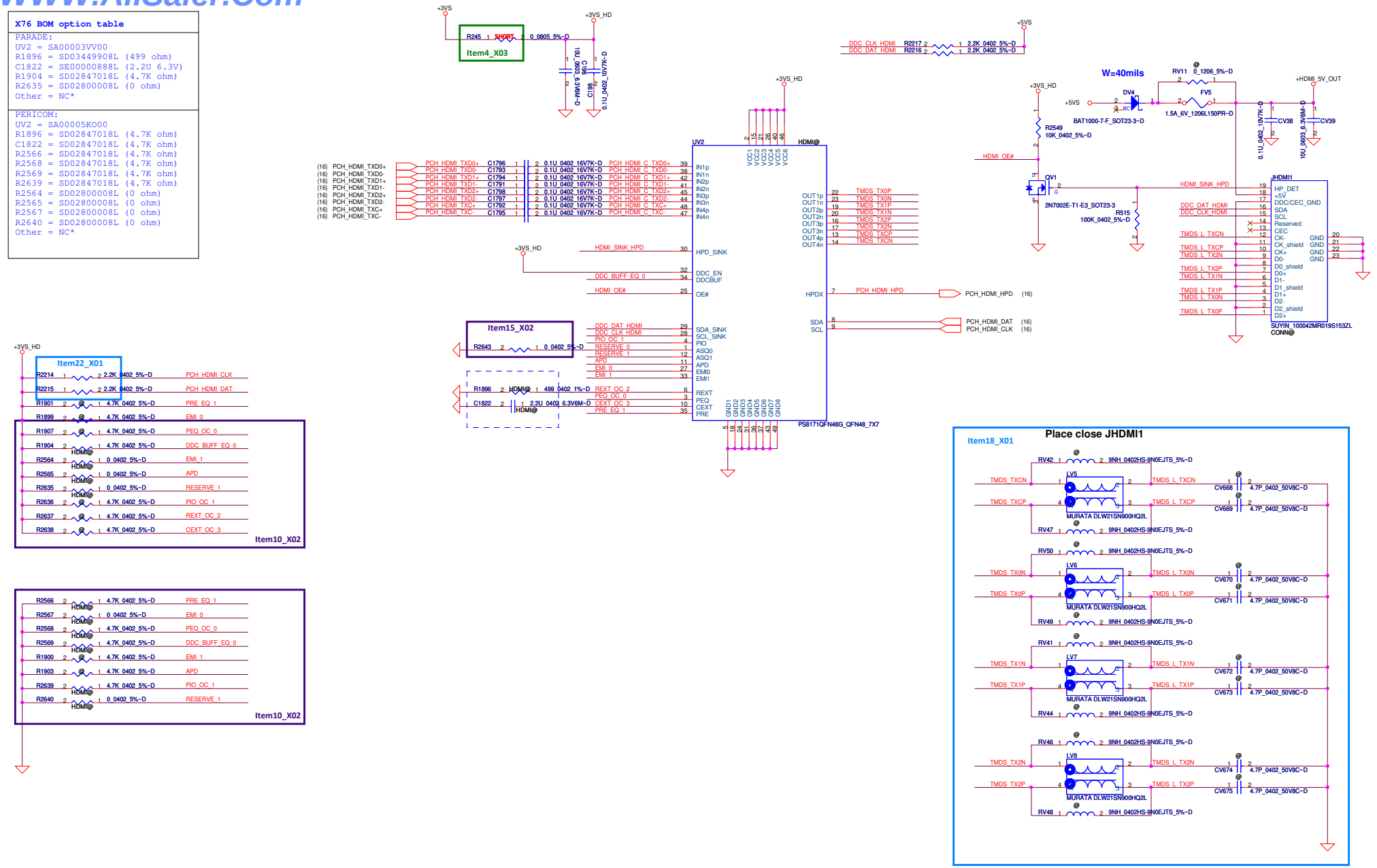
X76 BOM option table

PARADE:
UV2 = SA00003VV00
R1896 = SD03449908L (499 ohm)
C1822 = SE00000888L (2.2U 6.3V)
R1904 = SD02847018L (4.7K ohm)
R2635 = SD02800008L (0 ohm)
Other = NC*

PERICOM:
UV2 = SA00005KO00
R1896 = SD02847018L (4.7K ohm)
C1822 = SD02847018L (4.7K ohm)
R2566 = SD02847018L (4.7K ohm)
R2568 = SD02847018L (4.7K ohm)
R2569 = SD02847018L (4.7K ohm)
R2639 = SD02847018L (4.7K ohm)
R2564 = SD02800008L (0 ohm)
R2565 = SD02800008L (0 ohm)
R2567 = SD02800008L (0 ohm)
R2640 = SD02800008L (0 ohm)
Other = NC*



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.			
Title: HDMI SW			
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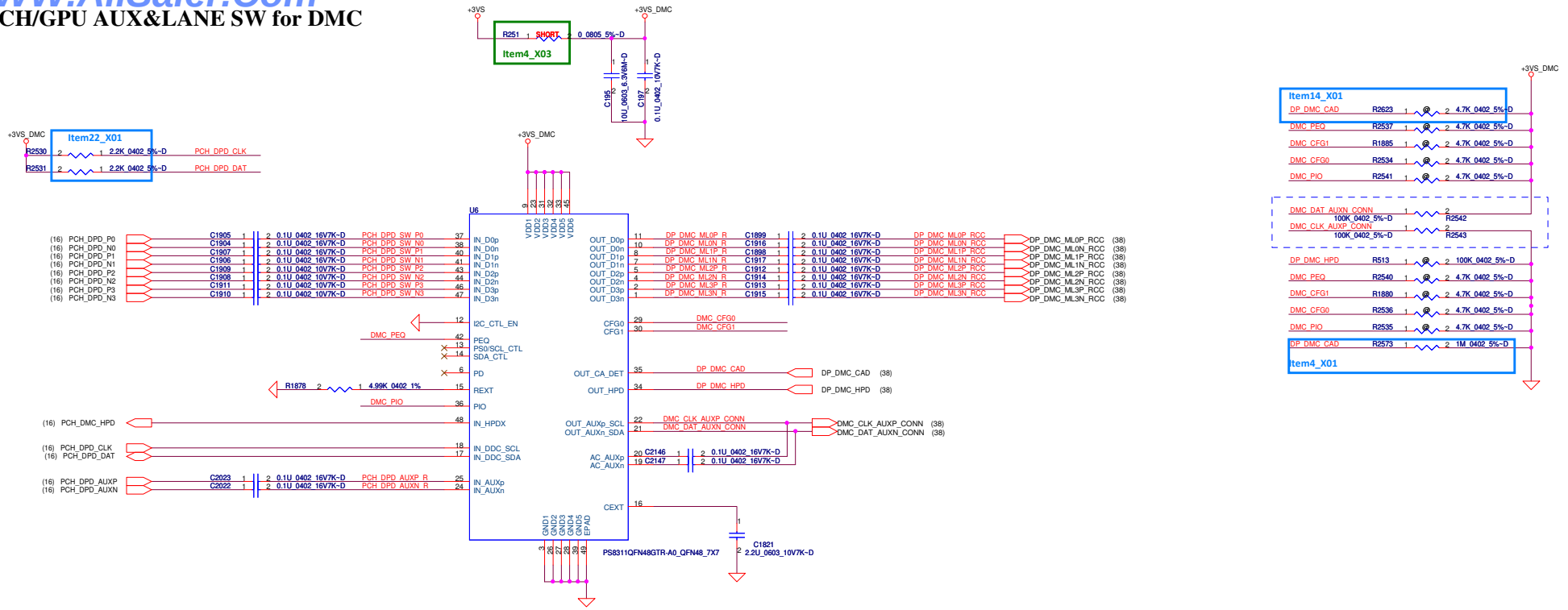
PCH/GPU AUX&LANE SW for DMC



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.			
Title	DMC MUX/Redriver		
Size C	Document Number LA-8381P		Rev 1.0
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X76 BOM option table

PERICOM (PI3EQX6741):
U637 = SA00004H100
RS318 = SD02800008L (0 ohm)
Other = NC*

PARADE (PS8520B):
U637 = SA00004WF00
RS317 = SD02800008L (0 ohm)
RS320 = SD02800008L (0 ohm)
RS321 = SD02800008L (0 ohm)
Other = NC*

TI (SN75LVCP601RTJR):
U637 = SA00003ZX0L
RS310 = SD02800008L (0 ohm)
RS318 = SD02800008L (0 ohm)
RS320 = SD02800008L (0 ohm)
RS321 = SD02800008L (0 ohm)
Other = NC*

m-SATA ReDriver

110mA

U637 mSATA@
PI3EQX6741STZDEX_TQFN20_4X4

Item28_X01

U641
PI2DBS6212ZHEX TQFN 28P
Item33_X01

Item3_X02

SEL	Source
0	SATA
1	PCIe

BlueTooth

Item31_X01
Item13_X02

To DMC PCB connector

mSATA_DET pin at pin 50

JWDB1
HRS_DF12(3.0)-80DP-0.5V86
CONN@

Item17_X03
330U_D2E_6.3VM_R25~D

Reserve for RF please close to JWDB1

Reserve for RF please close to JWDB1

SIM card board 4.7uF change to 1uF for Tiger detect issue.

SIM Connector

Item8_X03
JSIM1 CONN@
MOLEX_475531001~D

Item16_X02
IP4223CZ6_SO6~D

Reserve for SIM card does not meet rise time and pull-up is needed.

For ESD

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Compal Electronics, Inc.

Title: Mini Card -WLAN / DMC / BT

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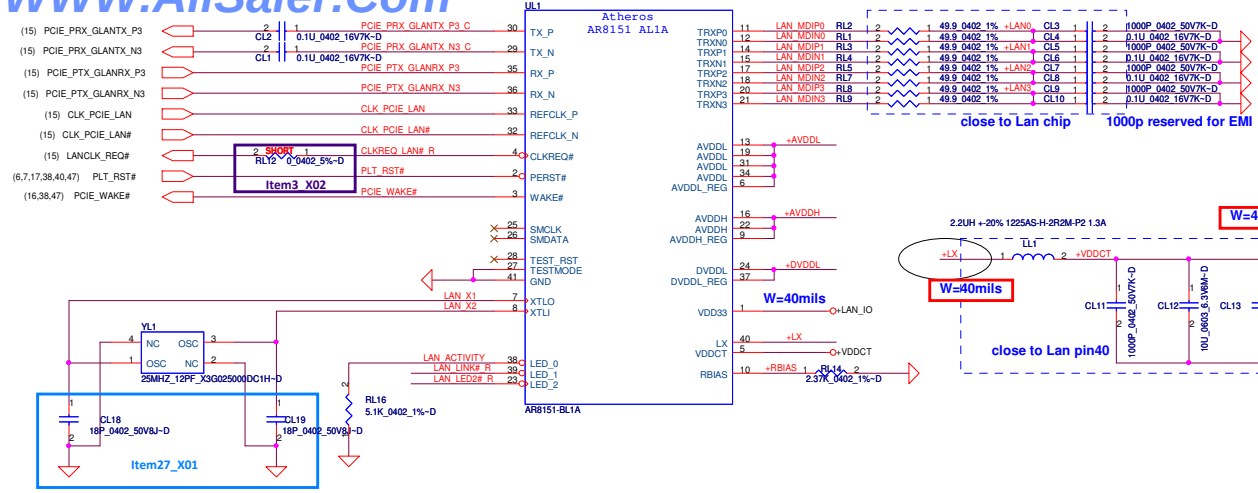

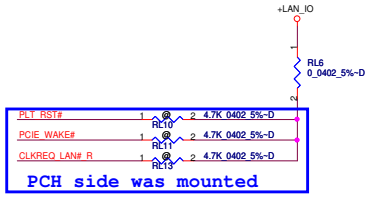

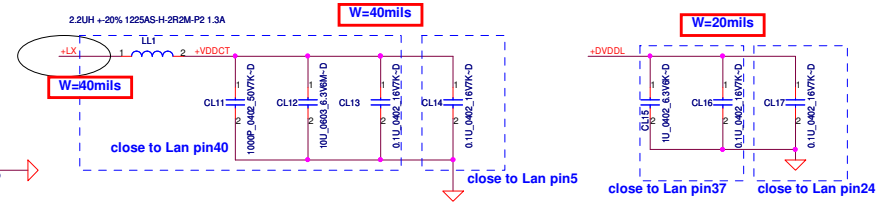

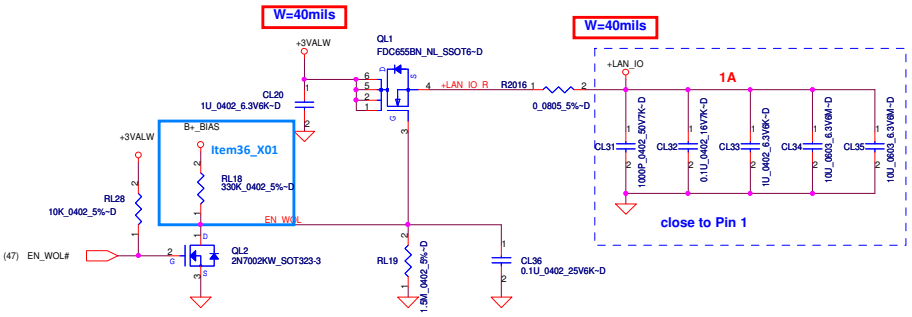

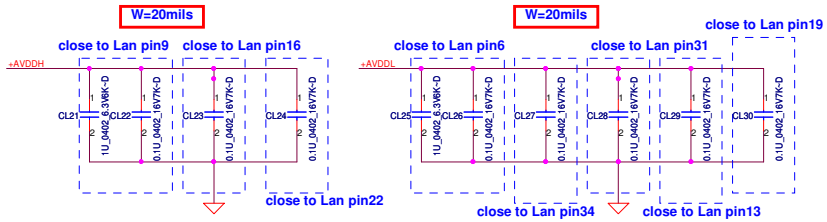

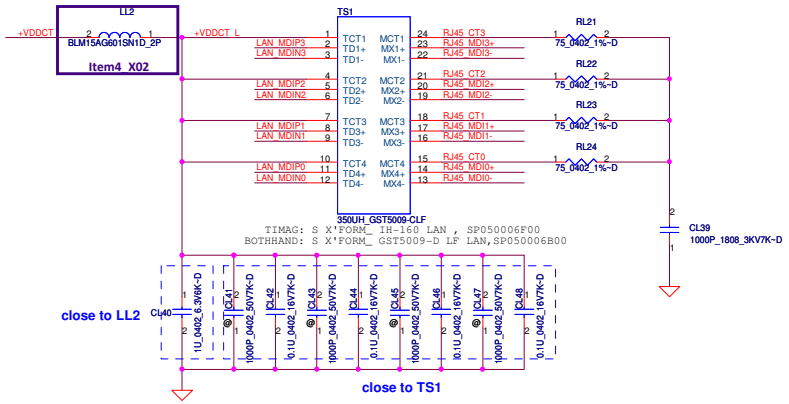

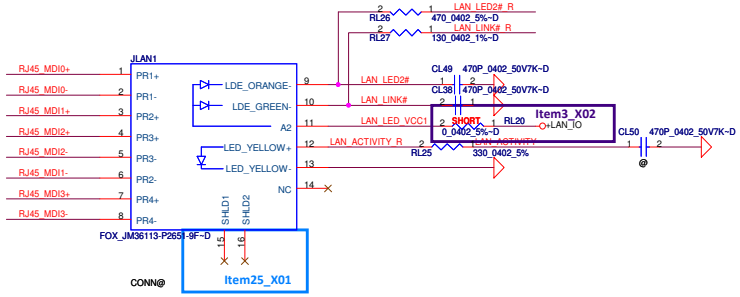

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.			
Title	GLAN AR8151 AL1A/ RJ45		
Size	Document Number		Rev
	LA-8381P		1.0
Date:	Thursday, January 12, 2012	Sheet	39 of 63

Item4_X03
+3VS — R2017 SHORT 0_0805_5%~D — +3VS_CR

check IC support 9 in 1 function

Zdiff = 100 ohm

U135

(15) PCIE_PTX_CARDRX_P4 — PCIE_PTX_CARDRX_P4 — HSIP
(15) PCIE_PTX_CARDRX_N4 — PCIE_PTX_CARDRX_N4 — HSIN
(15) CLK_PCIE_CD — CLK_PCIE_CD — REFCLKP
(15) CLK_PCIE_CD# — CLK_PCIE_CD# — REFCLKN
CR24 4.7U_0603_6.3V6K-D — AV12 — AV12
(15) PCIE_PRX_CARDTX_P4 — CR15 0.1U_0402_10V7K-D — PCIE_PRX_CARDTX_P4_C — HSOP
(15) PCIE_PRX_CARDTX_N4 — CR16 0.1U_0402_10V7K-D — PCIE_PRX_CARDTX_N4_C — HSON
GND
+ODR_PWR — CR22 0.1U_0402_10V7K-D — DV12 — DV12
Card1_3V3
+3VS_CR — 3V3_IN
Card2_3V3
XD_CD# — XD_CD#
DV33_18
GND
SP1_SDD7_XDRDY — SP1
SP2_SDD6_XDRE# — SP2
SP3_SDD5_XDCE# — SP3
SP4_SDD4_XDWE# — SP4
SD_D1_R — RR20 SHORT 0_0402_5%~D — SD_D1
SD_D0_R — RR19 SHORT 0_0402_5%~D — SD_D0
SD_CLK_R — RR23 33_0402_1% — SD_CLK
SD_CMD_R — RR24 SHORT 0_0402_5%~D — SD_CMD
SD_D3_R — RR21 SHORT 0_0402_5%~D — SD_D3

RREF — R1563 6.2K_0402_1%~D — +3VS_CR
3V3_IN — CR27 0.1U_0402_10V7K-D
CDCLK_REQ# — CDCLK_REQ# (15)
PLT_RST# — PLT_RST# (6,7,17,38,39,47)
EEDO
EECS
EESK
GPIO/EEDI
MS_INS# — MS_INS#
SD_CD# — SD_CD#
SP15_SDWP_XDD7
SP14_MSCLK_XDD6 — Item3_X02 SHORT RR22 0_0402_5%~D — SP14_MSCLK_XDD6_R — @ CR26 5P_0402_50V8C~D
SP13_MSD7_XDD5
SP12_MSD3_XDD4
SP11_MSD6_XDD3
SP10_MSD2_XDD2
SP9_MSD0_XDD1
SP8_MSD4_XDD0
SP7_MSD1_XDWP#
SP6_MSD5_XDALE
SP5_MSBS_XDCLE
DV12_S
GND
SD_D2 — CR21 0.1U_0402_10V7K-D — CR20 4.7U_0603_6.3V6K-D — RR12 SHORT 0_0402_5%~D — SD_D2_R

Item3_X02

Removed CR17

CR28 10U_0603_6.3V6M-D — CR19 0.1U_0402_10V7K-D — CR23 0.1U_0402_10V7K-D

@ CR25 5P_0402_50V8C-D Reserved

RTS5209-GR_LQFP48_7X7

+ODR_PWR
RR3 10K_0402_5%~D
CR3 0.1U_0402_10V7K-D
CR4 10U_0603_6.3V6M-D
CR5 0.1U_0402_10V7K-D
CR6 0.1U_0402_10V7K-D
For ver:ES2.0A

Place CR3 close to socket pin 22
Place CR4 close to socket pin 11
Place CR5 close to socket pin 11
Place CR6 close to socket pin 18

JREAD CONN@ T-SOL_144-1300002600_NR

+ODR_PWR
XD-VCC
XD10-D0
XD11-D1
XD12-D2
XD13-D3
XD14-D4
XD15-D5
XD16-D6
XD17-D7
XD07-WE
XD08-WP
XD06-ALE
XD01-CD
XD02-R/B
XD03-RE
XD04-CE
XD05-CLE
XD GND
XD GND
SD CD/WP GND
SD CD/WP GND

SD4-VDD
MS9-VCC
SD5-CLK — SD_CLK_R
SD7-DAT0 — SD_D0_R
SD8-DAT1 — SD_D1_R
SD9-DAT2 — SD_D2_R
SD1-DAT3 — SD_D3_R
SD2-CMD — SD_CMD_R
SD-CD — SD_CD#
SD-WP — SP15_SDWP_XDD7
SD6-VSS
SD3-VSS
MS8-SCLK — SP14_MSCLK_XDD6_R
MS4-DATA0 — SP9_MSD0_XDD1
MS3-DATA1 — SP7_MSD1_XDWP#
MS5-DATA2 — SP10_MSD2_XDD2
MS7-DATA3 — SP12_MSD3_XDD4
MS6-INS — MS_INS#
MS2-BS — SP5_MSBS_XDCLE
MS1-VSS
MS10-VSS

Reserve for EMI please close to JREAD1
@ RR8 33_0402_5%~D — @ CR14 22P_0402_50V8J~D

Reserve for EMI please close to JREAD1
@ RR11 33_0402_5%~D — @ CR18 22P_0402_50V8J~D

Co-lay connector for 2nd. 2010/11/26

+ODR_PWR
JREAD1 CONN@ ALPS_SCDG4B0102_NR

XD-VCC
XD-D0
XD-D1
XD-D2
XD-D3
XD-D4
XD-D5
XD-D6
XD-D7
XD-WE
XD-WP
XD-ALE
XD-CD
XD-R/-B
XD-RE
XD-CE
XD-CLE
XD-GND
XD-GND
GND
GND

SD-VDD/MMC-VDD
MS-VCC
MMC-CLK/SD-CLK
MMC-DAT/SD-DAT0
SD-DAT1
SD-DAT2
MMC-RSV/SD-DAT3
SD-CMD/MMC-CMD
SD-CD
SD-WP
SD-CD
MS-SCLK
MS-SDIO/DATA0
MS-DATA1
MS-DATA2
MS-DATA3
MS-INS
MS-BS
MS-VSS
MS-VSS
SD-VSS/MMC-VSS1
SD-VSS/MMC-VSS2
SD-VSS/MMC-VSS2

SD_CLK_R
SD_D0_R
SD_D1_R
SD_D2_R
SD_D3_R
SD_CMD_R
SD_CD#
SP15_SDWP_XDD7
SP14_MSCLK_XDD6_R
SP9_MSD0_XDD1
SP7_MSD1_XDWP#
SP10_MSD2_XDD2
SP12_MSD3_XDD4
MS_INS#
SP5_MSBS_XDCLE

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: Card Reader RTS5209

Size	Document Number	Rev
	LA-8381P	1.0

Date: Thursday, January 12, 2012 Sheet 40 of 63

PC BEEP

SENSE pin

Close to chip side

HeadPhone / Mic. combo JACK

Setting the Turn-Off Time:
Ton (ms) = 0.02 x Cset (pF)

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

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Compal Electronics, Inc.

Title: Codec Malcolm-EX

Size: | Document Number: LA-8381P | Rev: 1.0

Date: Thursday, January 12, 2012 | Sheet 41 of 63

Line Out/HeadPhone

Mic. JACK

Int. Speaker Connector

Subwoofer support 3W

GAIN0	GAIN1	
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

W=40mil

W=20mil

Setting the Turn-Off Time:
Ton (ms) = 0.02 x Cset (pF)

20mil

ANPEC
APA2031RI-TRG
SA00001R210

ANPEC
APA0714XAI-TRG
SA000059X00

either one option.

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.

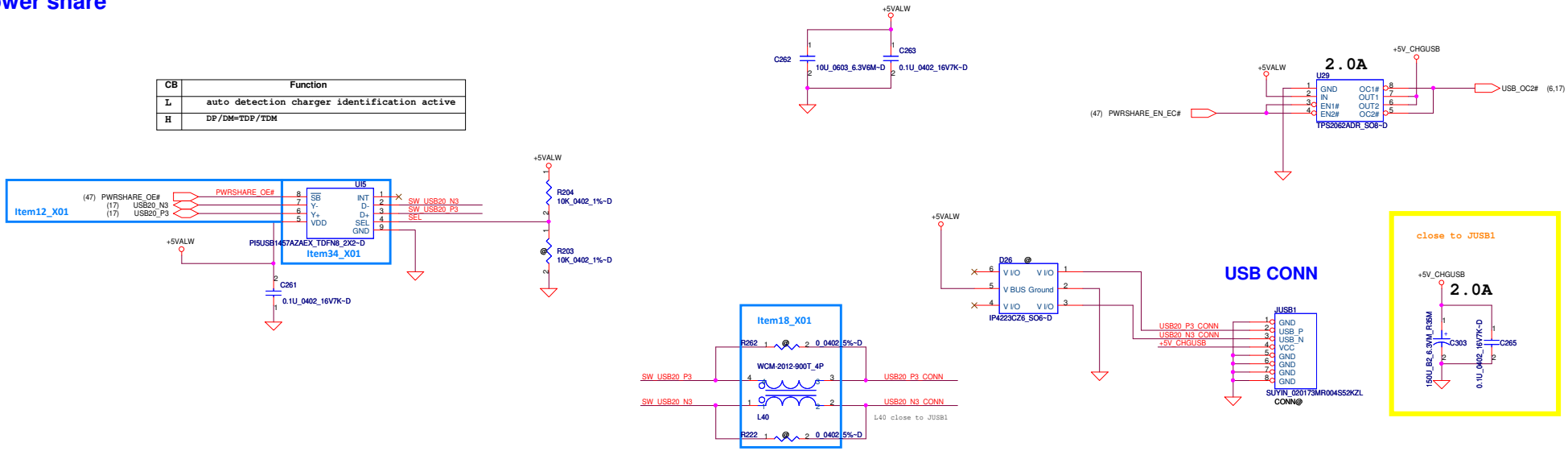
Title: Amp TPA6017/subwoofer/ Audio Jack

Size	Document Number	Rev
	LA-8381P	1.0

Date: Thursday, January 12, 2012 | Sheet 42 of 63

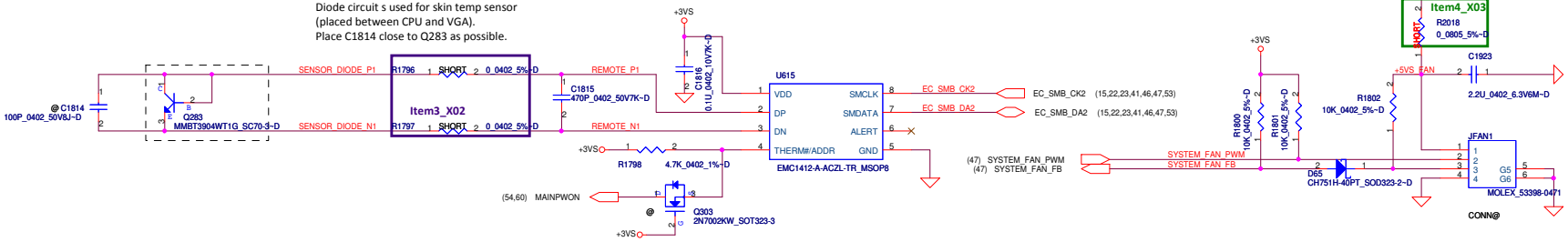
Power share

CB	Function
L	auto detection charger identification active
H	DP/DM=TDP/TDM



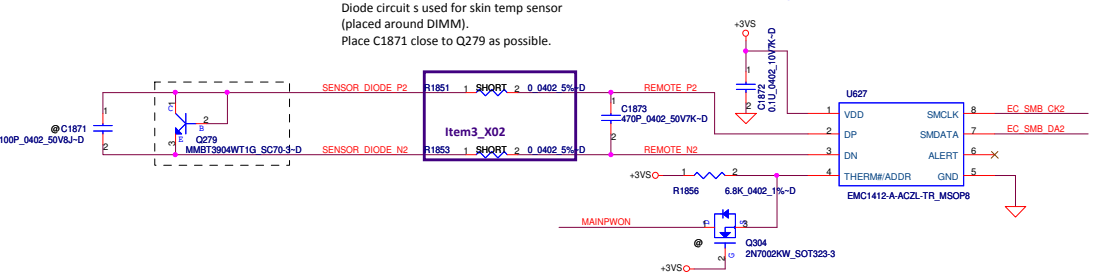
System Thermal Sensor 1

Diode circuit s used for skin temp sensor
(placed between CPU and VGA).
Place C1814 close to Q283 as possible.



System Thermal Sensor 2

Diode circuit s used for skin temp sensor
(placed around DIMM).
Place C1871 close to Q279 as possible.



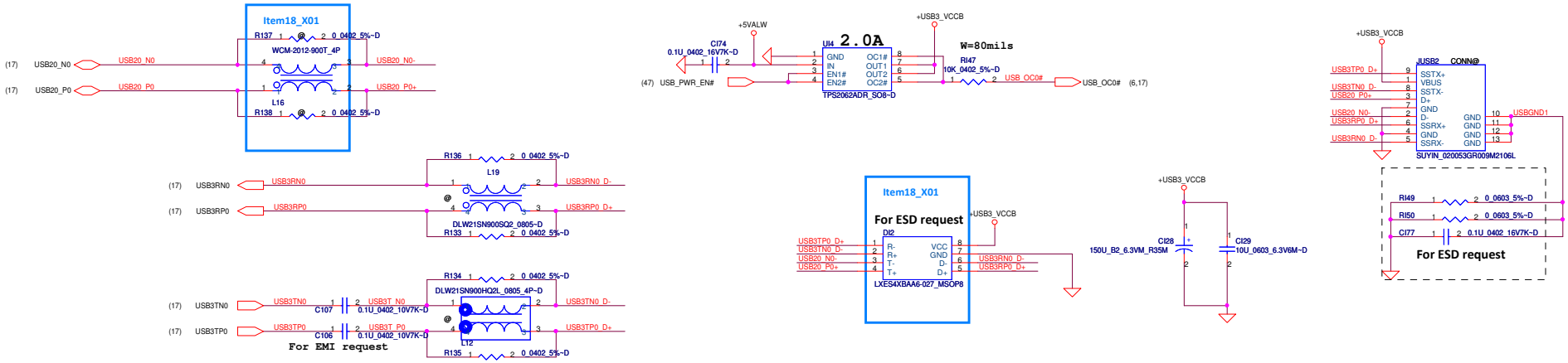
Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

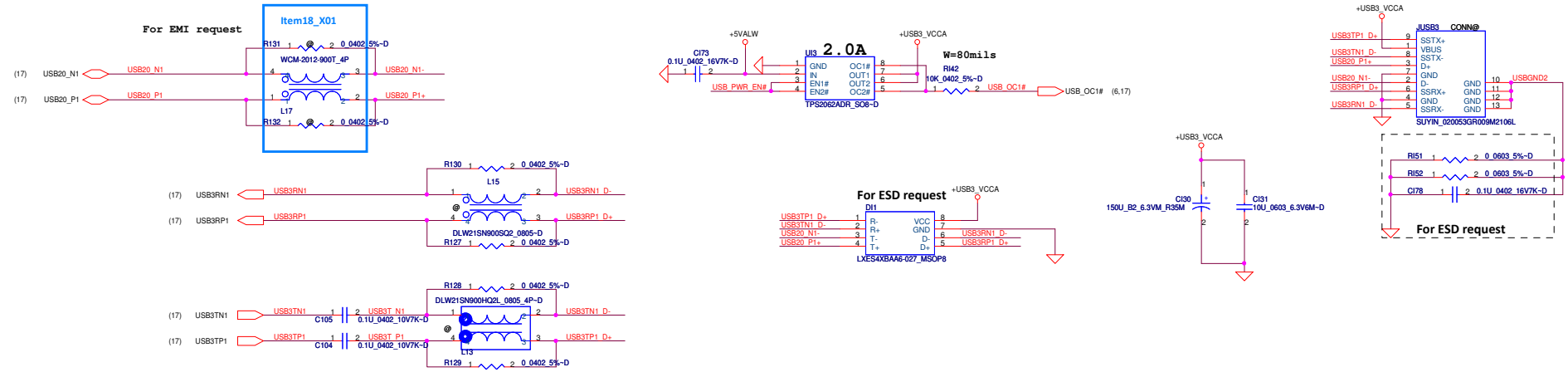
Compal Electronics, Inc.

Title: USB conn.

Size	Document Number	Rev
	LA-8381P	1.0

Date: Thursday, January 12, 2012 | Sheet 43 of 63

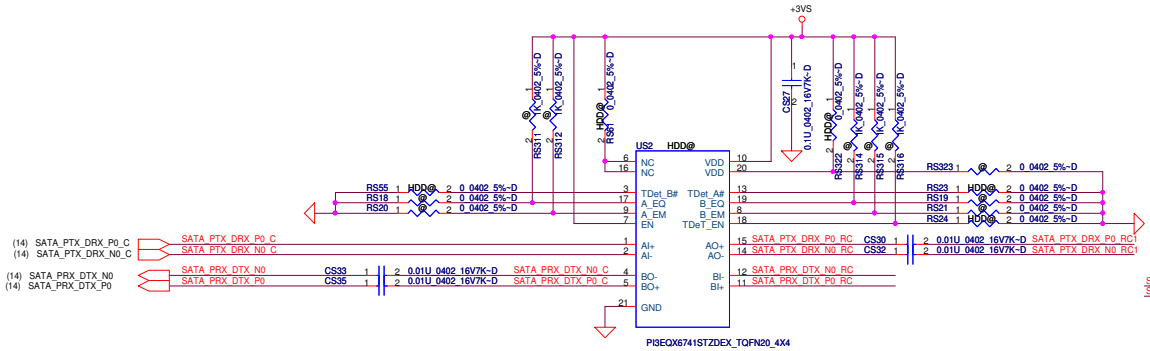


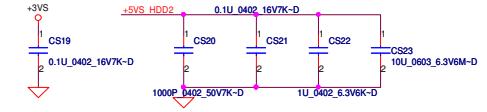


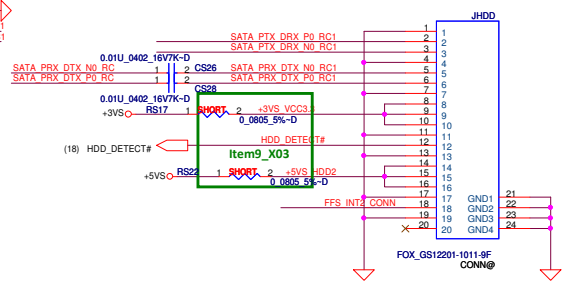
Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.			
Title: USB conn.			
Size	Document Number: LA-8381P		Rev: 1.0
Date: Thursday, January 12, 2012		Sheet 44 of 63	

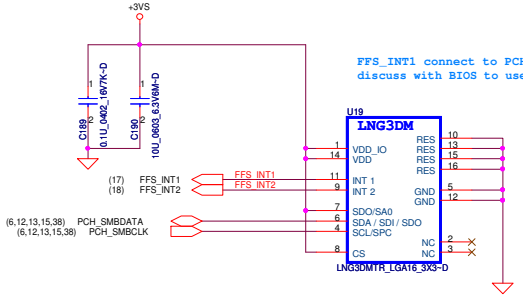
X76 BOM option table
PERICOM (PI3EQX6741): US2 = SA00004H100 RS322 = SD02800008L (0 ohm) Other = NC*
PARADE (PS8520B): US2 = SA00004WF00 RS23 = SD02800008L (0 ohm) RS55 = SD02800008L (0 ohm) RS61 = SD02800008L (0 ohm) Other = NC*
TI (SN75LVCP601RTJR): US2 = SA00003ZX0L RS23 = SD02800008L (0 ohm) RS24 = SD02800008L (0 ohm) RS55 = SD02800008L (0 ohm) RS322 = SD02800008L (0 ohm) Other = NC*



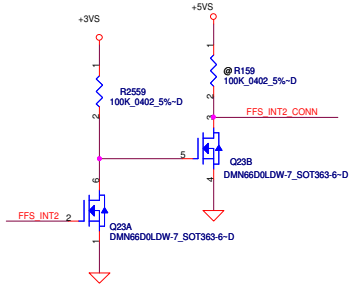




Free Fall Sensor

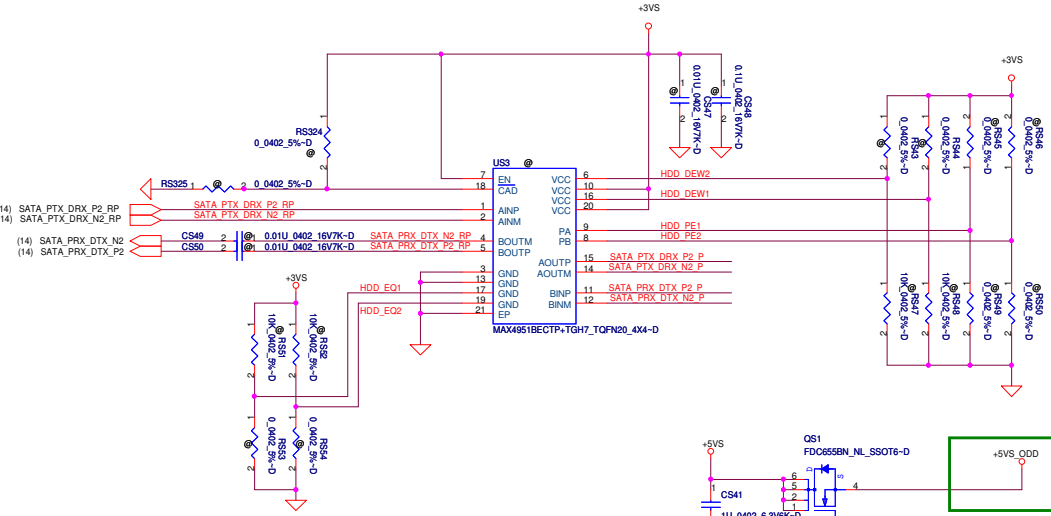


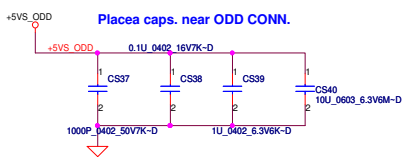
FFS_INT1 connect to PCH GPIO & EC discuss with BIOS to use which pin



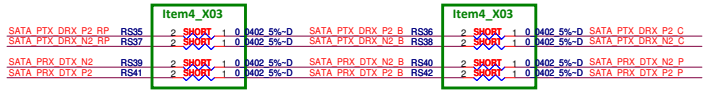
By Pass circuit

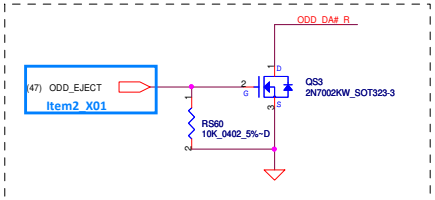
Item28_X01

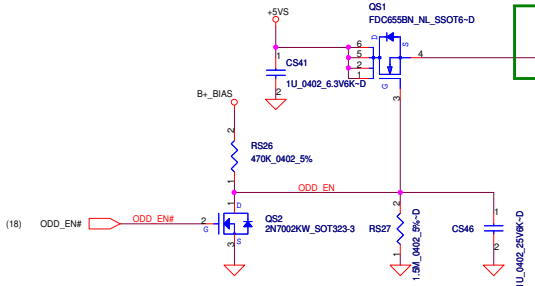


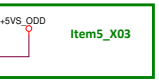


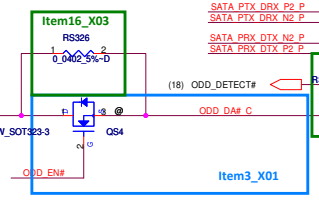
	MAXIM main	TI 2nd
P/N	SA00003LH1L	SA00003ZX0L
RS43 RS44	pop	depop
RS47 RS48	depop	pop
RS53 RS54	pop	depop



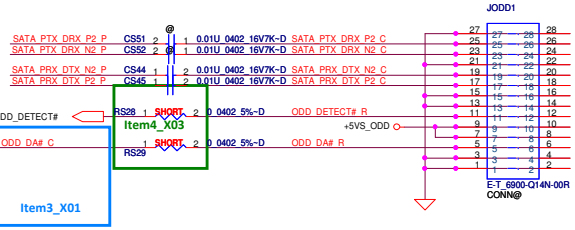








SATA ODD Conn.



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.			
Title: FFS /HDD/ ODD Connector			
Size	Document Number: LA-8381P		Rev: 1.0
Date: Thursday, January 12, 2012	Sheet 45 of 63		

Power Button

ON/OFF switch

TOP Side

SW6 SMT1-05-A 4P

Bottom Side

SW5 SMT1-05-A 4P

Test Only

ON/OFFBTN#

C326 0.1U_0402_25V6K-D

D28 PESD24VS2UT_SOT23-3-D

D27 DAN202UT106_SC70-3

+3VALW_EC

R263 100K_0402_5%-D

ON/OFF (47)

51ON# (52)

ON/OFFBTN# (49)

EC_ON (47,54)

R264 10K_0402_5%-D

Item13_X02

Q24 2N7002K_SOT23-3

Item23_X01

6251VDD

R2630 100K_0402_5%-D

Q310A DMN66D0LDW-7_SOT363-6-D

Q310B DMN66D0LDW-7_SOT363-6-D

BATT_TEMP (47,60)

ACIN (22,47,48,53)

Q311 2N7002E-T1-E3_SOT23-3

INT_KBD Conn.

KSI[0..7] KSO[0..16]

KB_DET# (47)

KB detect pin

CONN@ TYCO_3-2041084-0

JKB

VPK

U626 VPK@ MSP430F5508IRGCR_VQFN64_9X9

Item4_X03

CONN@ JKBBL2 TYCO_2-2041070-6-D

Analog Keys

Item13_X01

Item13_X01

K/B Backlight CONN (co-lay VPK)

JKBBL1 TYCO_1-2041070-6-D CONN@

F3 0.5A_13.2V_NANOSMDC050F-13.2-2

1Mb SPI ROM

U38 @ MX25L1006EMI-10G SOP 8P

24MHZ_12PF_7V24000020

FD1 FD2 FD3 FD4 FIDUCIAL_C40M80

CLIP1 CLIP2 CLIP3 EMI_CLIP CONN@

ZZZ1 PCB-MB

8/17

1, Analog keys connector and F/P temporary use.

2, check pin assignment.

3, check VPK K/B layout.

Reserve for EMI please close to U48

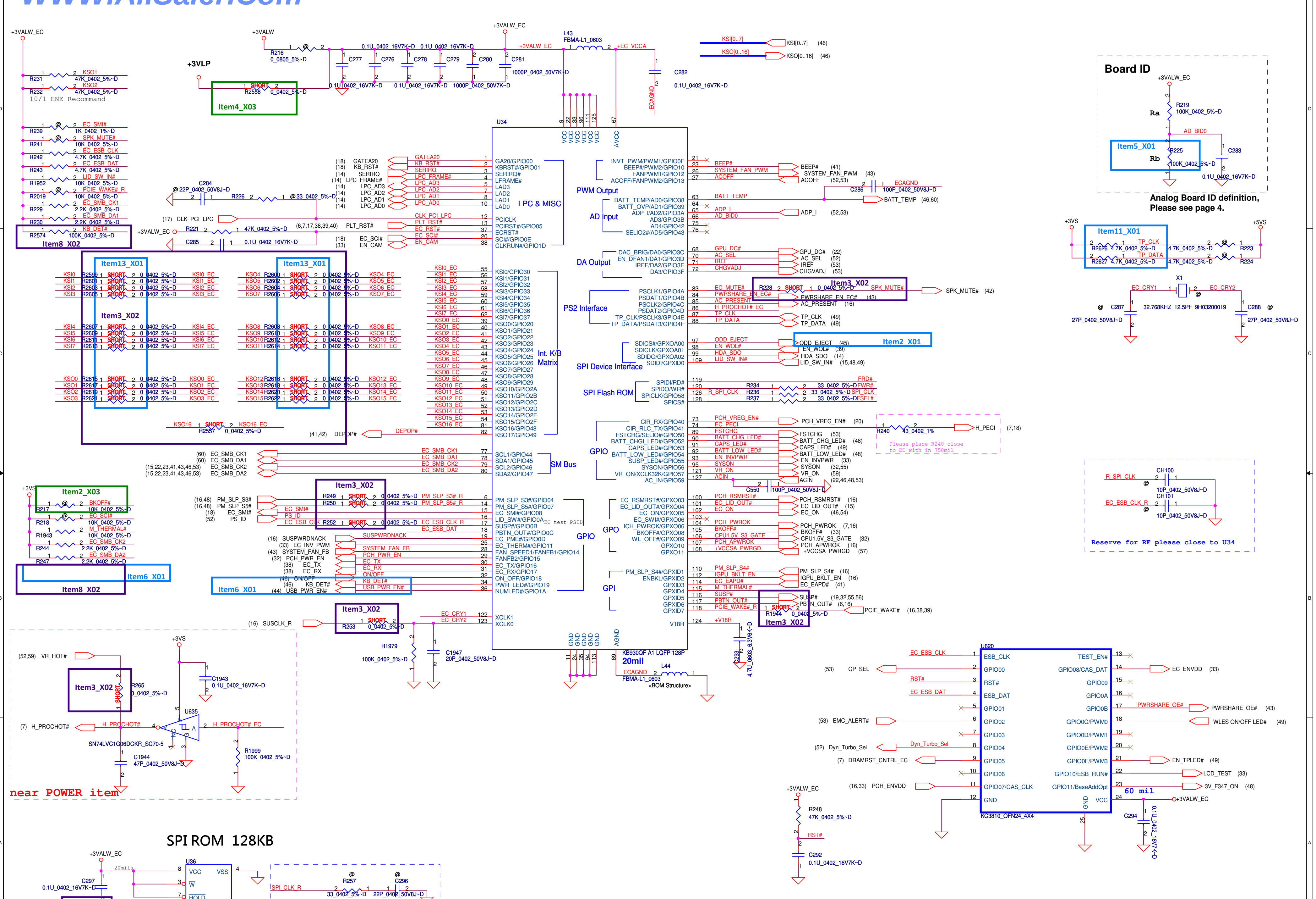
Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: PWRBTN/SCREWH/KB

Size: | Document Number: LA-8381P | Rev: 1.0

Date: Thursday, January 12, 2012 | Sheet 46 of 63



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

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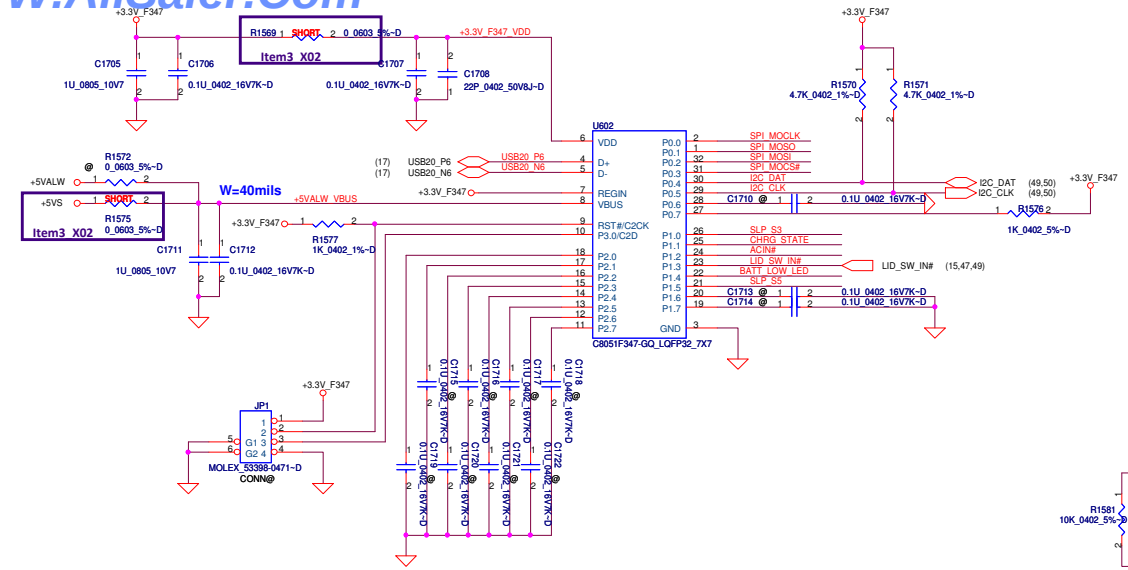
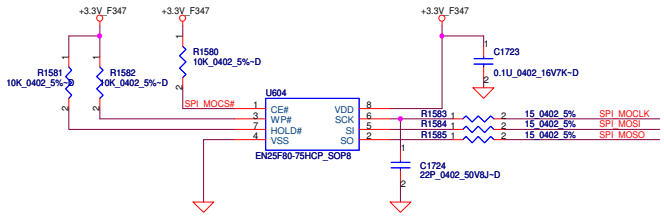
Compal Electronics, Inc.

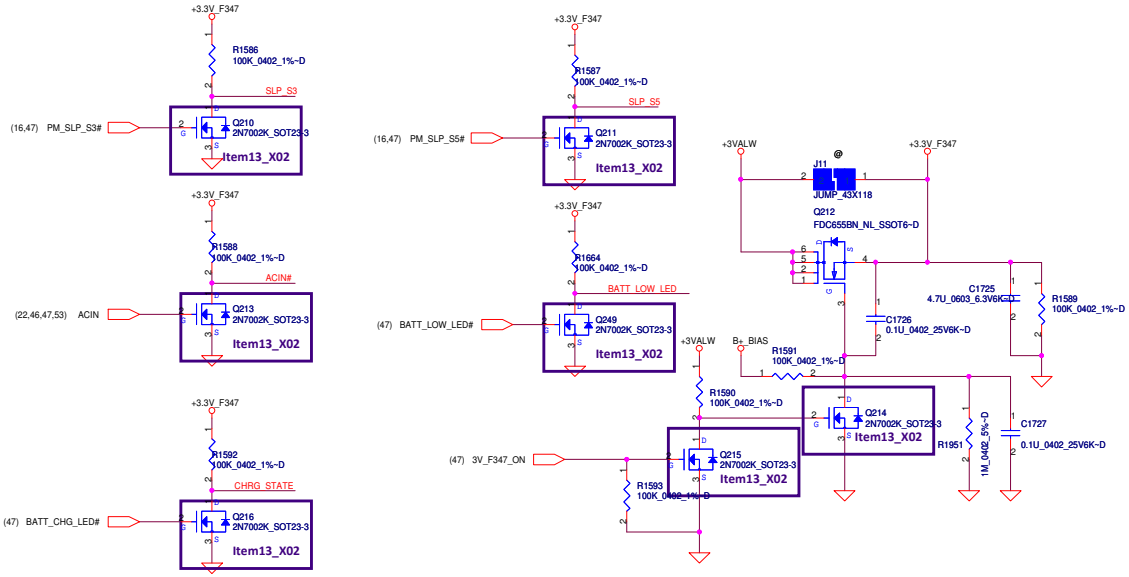
Title: EC ENE-KB930/ ENE3810

Size | Document Number: LA-8381P | Rev: 1.0

Date: Thursday, January 12, 2012 | Sheet 47 of 63







+3.3V_F347 behavior

	STATE			
	S0	S3	S4	S5
AC IN	ON	ON	ON	ON
BAT only	ON	ON	OFF	OFF

DEVICE	SMBUS ADDRESS
MAXIM - LED	0100 000b
MAXIM - GPIO	0100 001b
I2C EEPROM	1010 000b

AC mode battery full in S5:turn off ELC controller

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

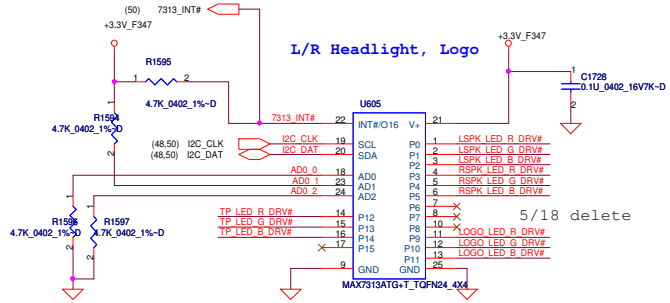
Compal Electronics, Inc.

Title: ELC (1)/STATUS CONN

Size	Document Number	Rev
	LA-8381P	1.0

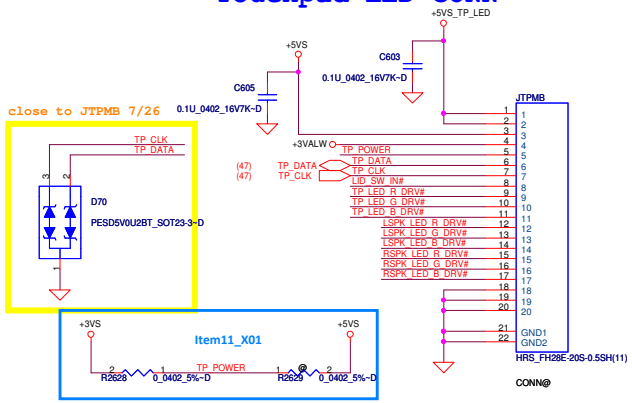
Date: Thursday, January 12, 2012 Sheet 48 of 63

L/R Headlight, Logo

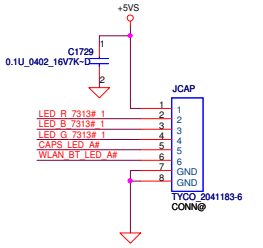


5/18 delete

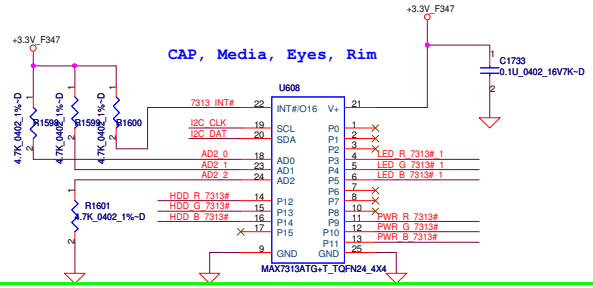
Touchpad LED CONN



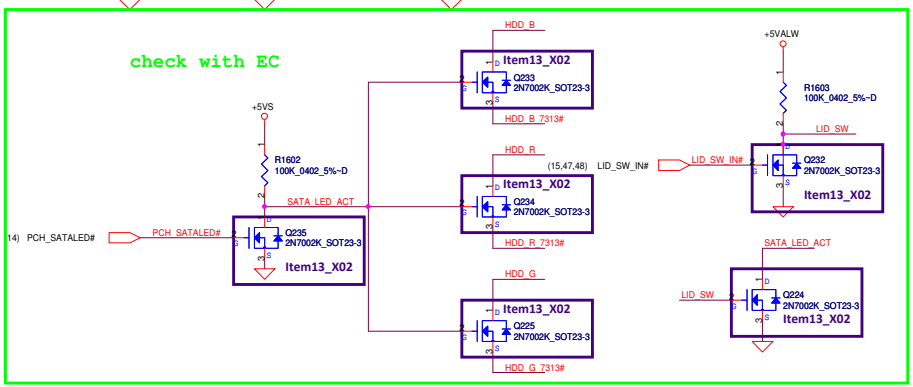
Indicator CONN

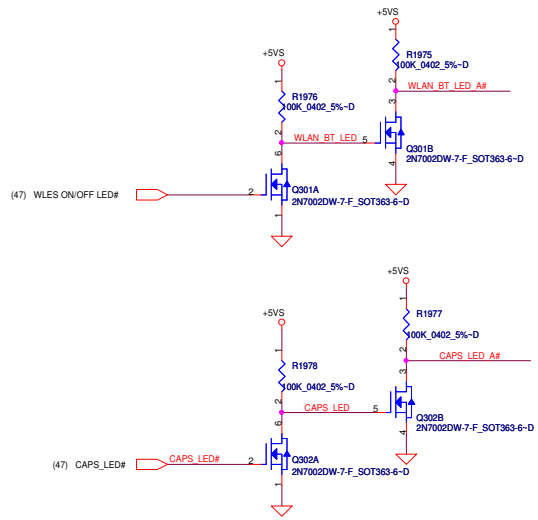


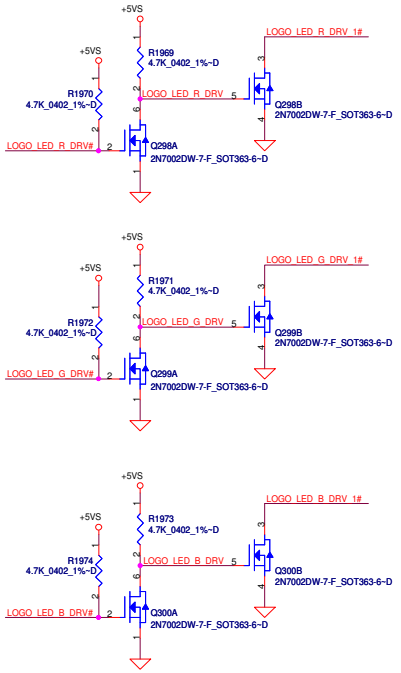
CAP, Media, Eyes, Rim



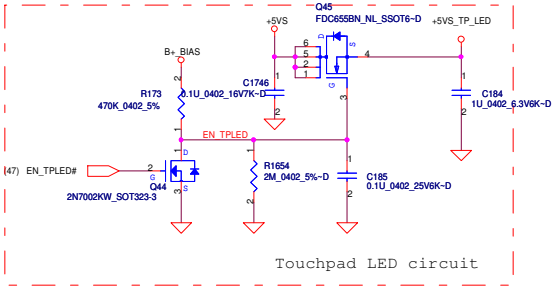
check with EC



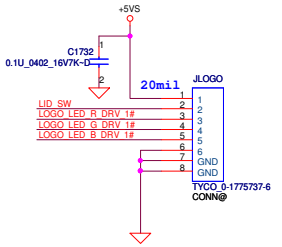




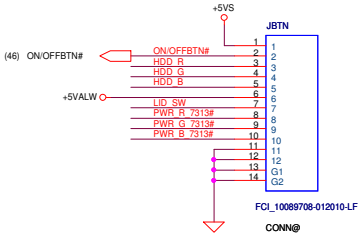
Reference	AD2	AD1	AD0	MAX7313
U605	0	1	0	L/R Headlight , Logo, TP
U608	0	1	1	Num, CAP , SCR EJECT, REV, PLAY/PAUSE FFWD, Vol_DWN, Vol_UP Wireless ON/OFF AWCC Button Alien Adrenaline Power Button Eyes Power Button Rim



LOGO Board CONN



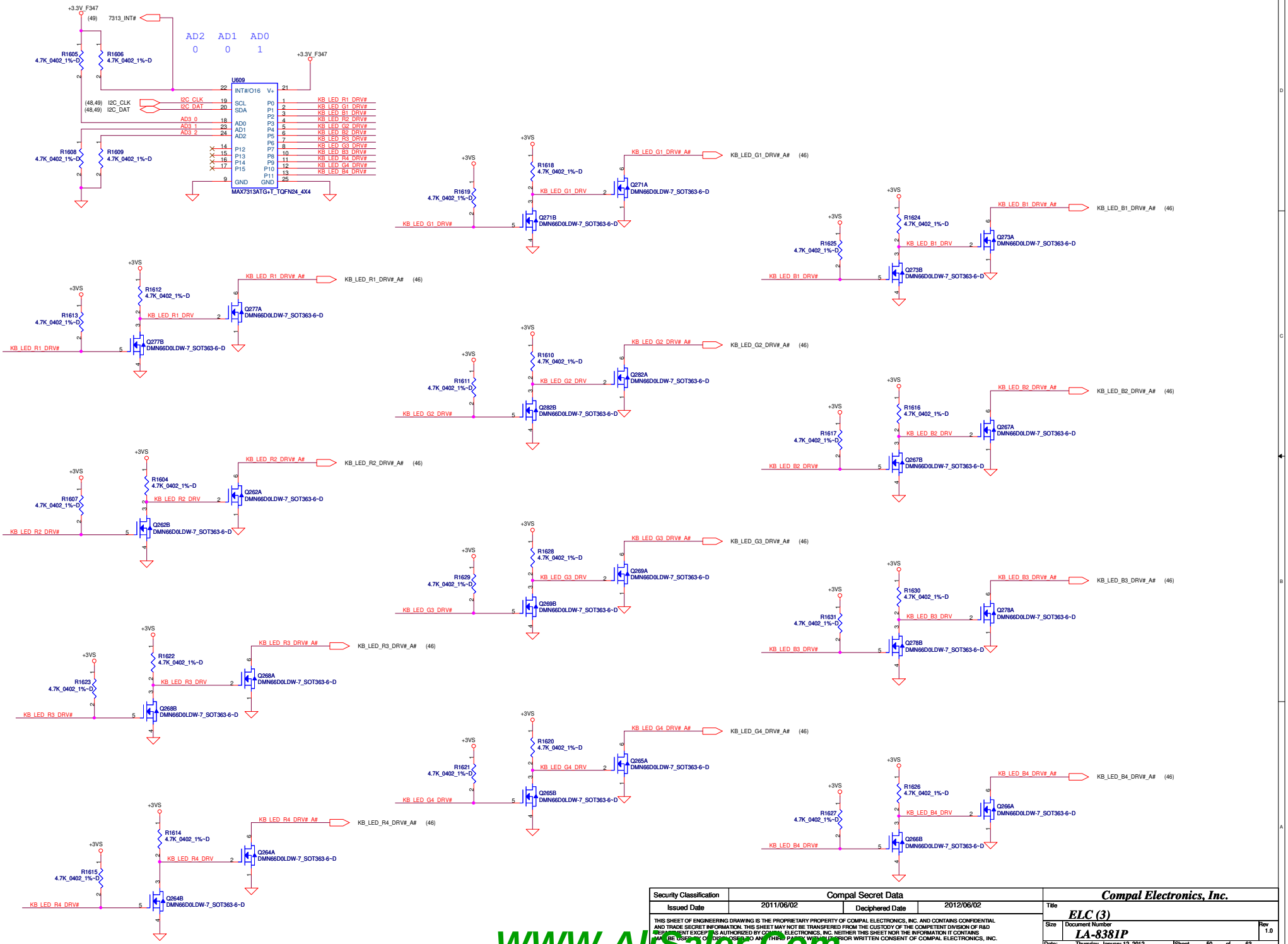
PWR BTN Board CONN



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.			
Title: ELC (2)			
Size	Document Number: LA-8381P		Rev: 1.0
Date: Thursday, January 12, 2012	Sheet 49 of 63		

K/B Backlight



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

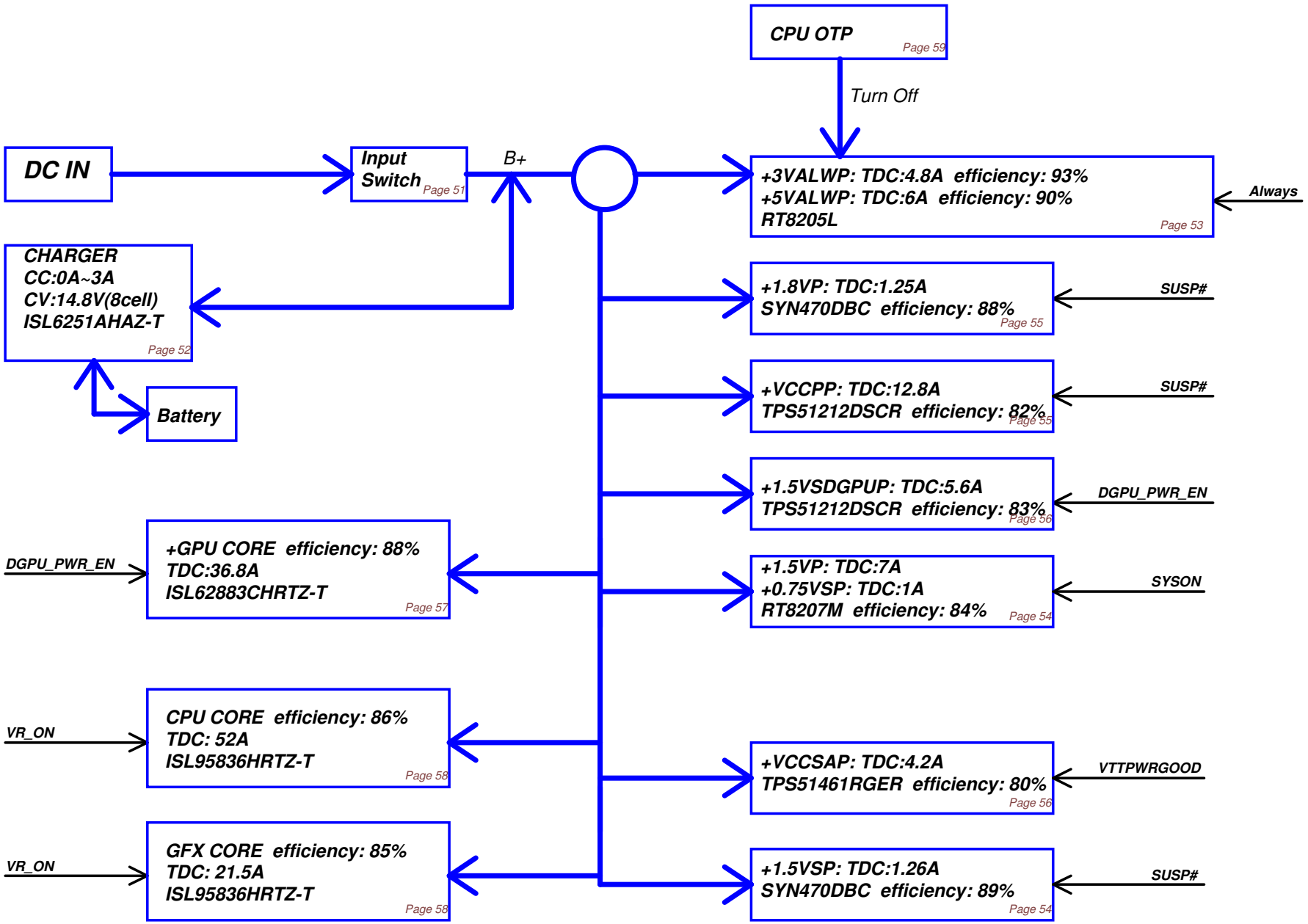
Compal Electronics, Inc.

Title: ELC (3)

Size	Document Number	Rev
	LA-8381P	1.0

Date: Thursday, January 12, 2012 Sheet 50 of 63

Power block



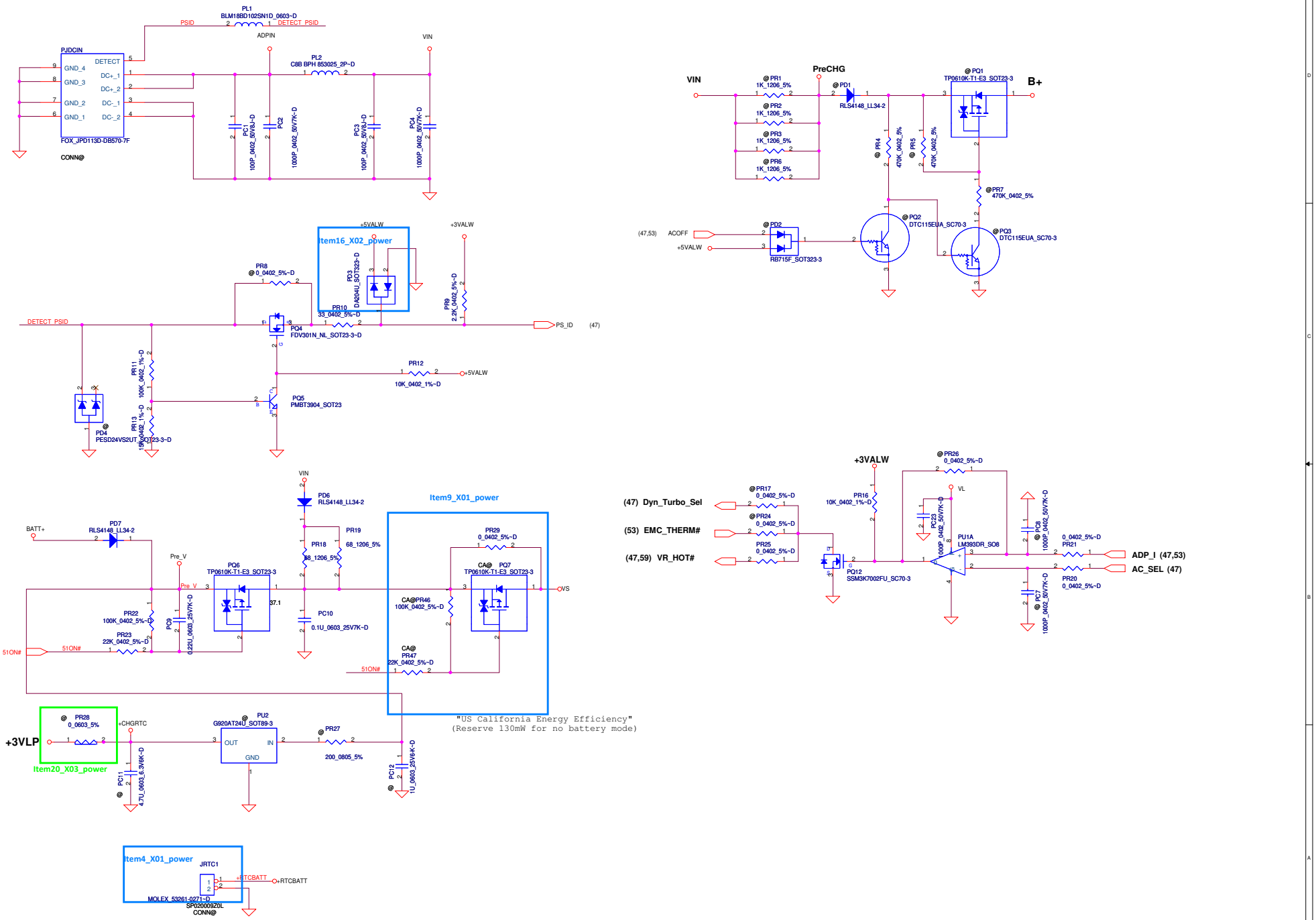
Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: POWER BLOCK DIAGRAM

Size	Document Number	Rev
Custom	LA-6801P	1.0

Date: Thursday, January 12, 2012 Sheet 51 of 63



Security Classification	Compal Secret Data		
Issued Date	2011/01/31	Deciphered Date	2012/01/31

Compal Electronics, Inc.

Title: PWR-DCIN / Vin Detector

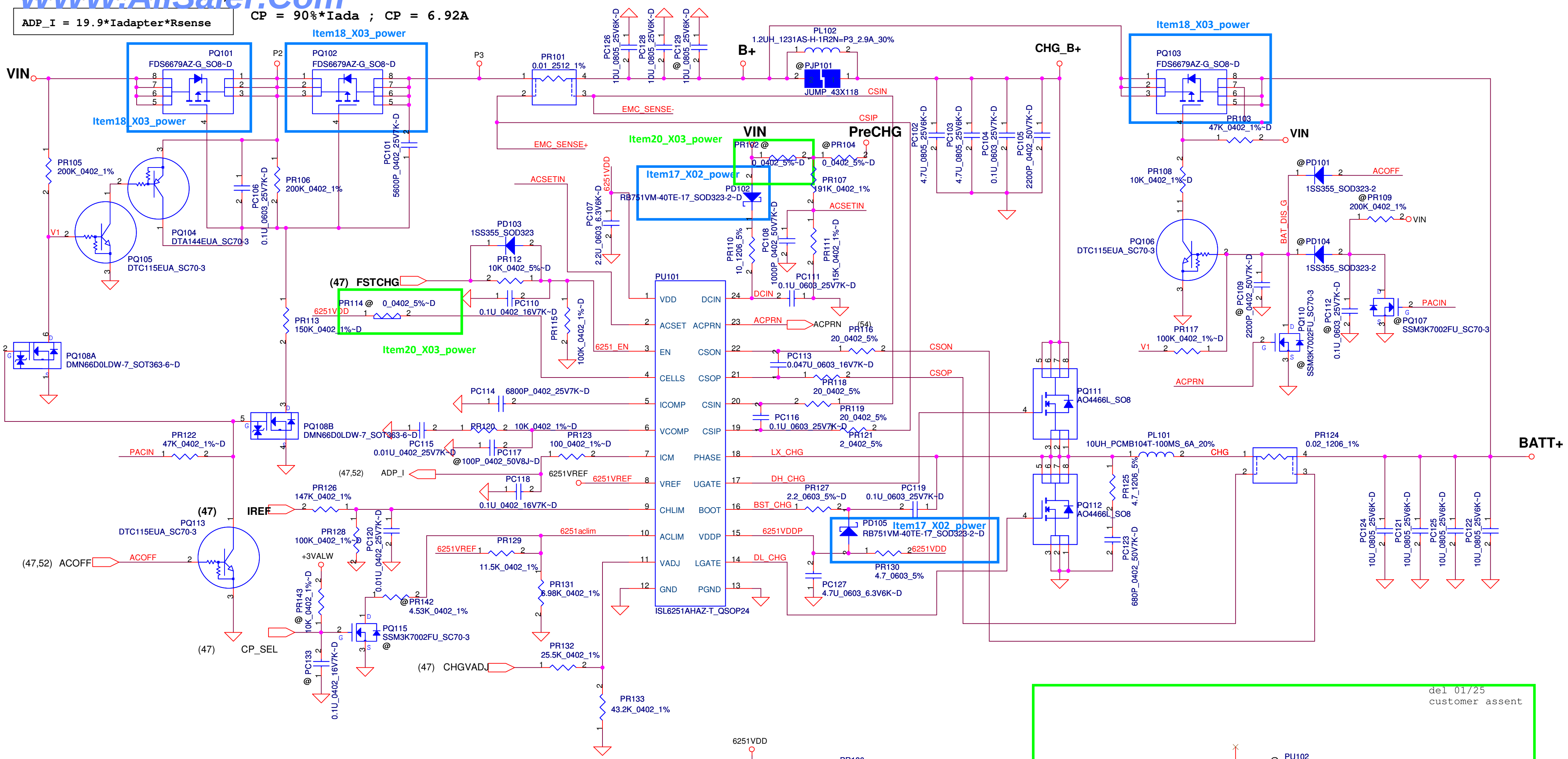
Size	Document Number	Rev
C	LA-8381P	0.1

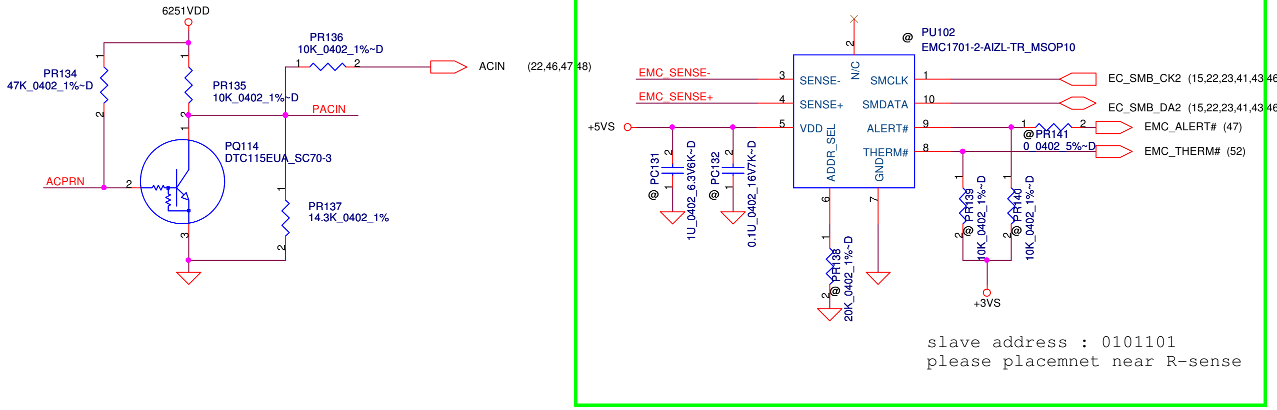
Date: Thursday, January 12, 2012 | Sheet 52 of 63

Iada=0.7~69.4 150W/19.5V=7.69A)

ADP_I = 19.9*Iadapter*Rsense

CP = 90%*Iada ; CP = 6.92A





CP mode
Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)
Vaclim=2.39*((6.98K//152K)/((11.5K//152K)+(6.98K//152K))

CC=3.3A
IREF=1*Icharge
IREF=0.25V~3.3V

CHGVADJ	CV mode
0V	3.99V per cell
1.93V	4.2V per cell
3.3V	4.35V per cell

BATT Type	Charging Voltage (0x15)	CV mode
Normal 4S LI-ON Cells	14800mV	14.80V

Security Classification	Compal Secret Data		
Issued Date	2011/01/31	Deciphered Date	2012/01/31

Compal Electronics, Inc.

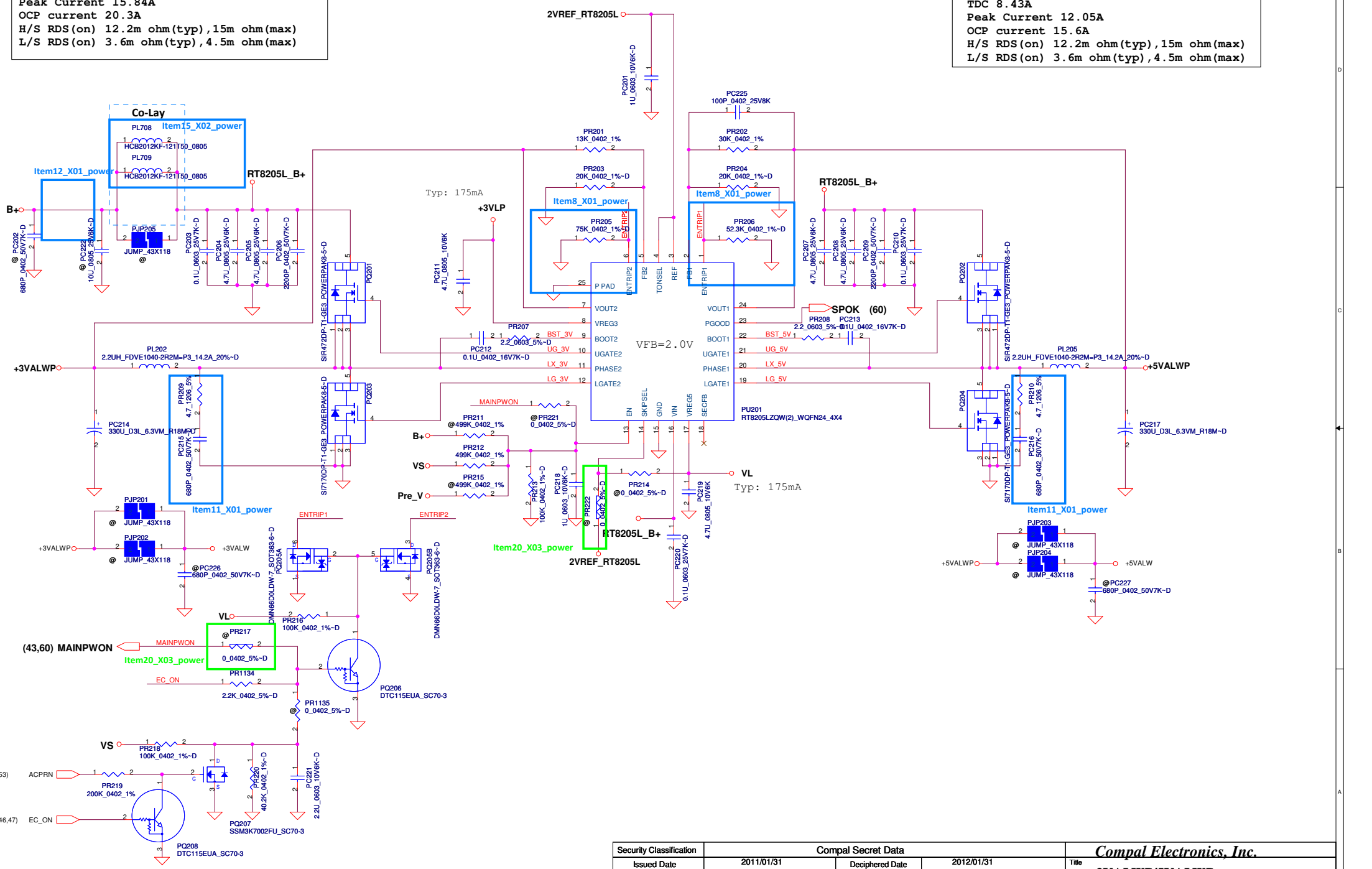
Title: *PWR-CHARGER*

Size: Custom | Document Number: *LA-8381P* | Rev: 1.0

Date: Thursday, January 12, 2012 |

3.3VALWP
TDC 11.09A
Peak Current 15.84A
OCP current 20.3A
H/S RDS(on) 12.2m ohm(typ),15m ohm(max)
L/S RDS(on) 3.6m ohm(typ),4.5m ohm(max)

5VALWP
TDC 8.43A
Peak Current 12.05A
OCP current 15.6A
H/S RDS(on) 12.2m ohm(typ),15m ohm(max)
L/S RDS(on) 3.6m ohm(typ),4.5m ohm(max)



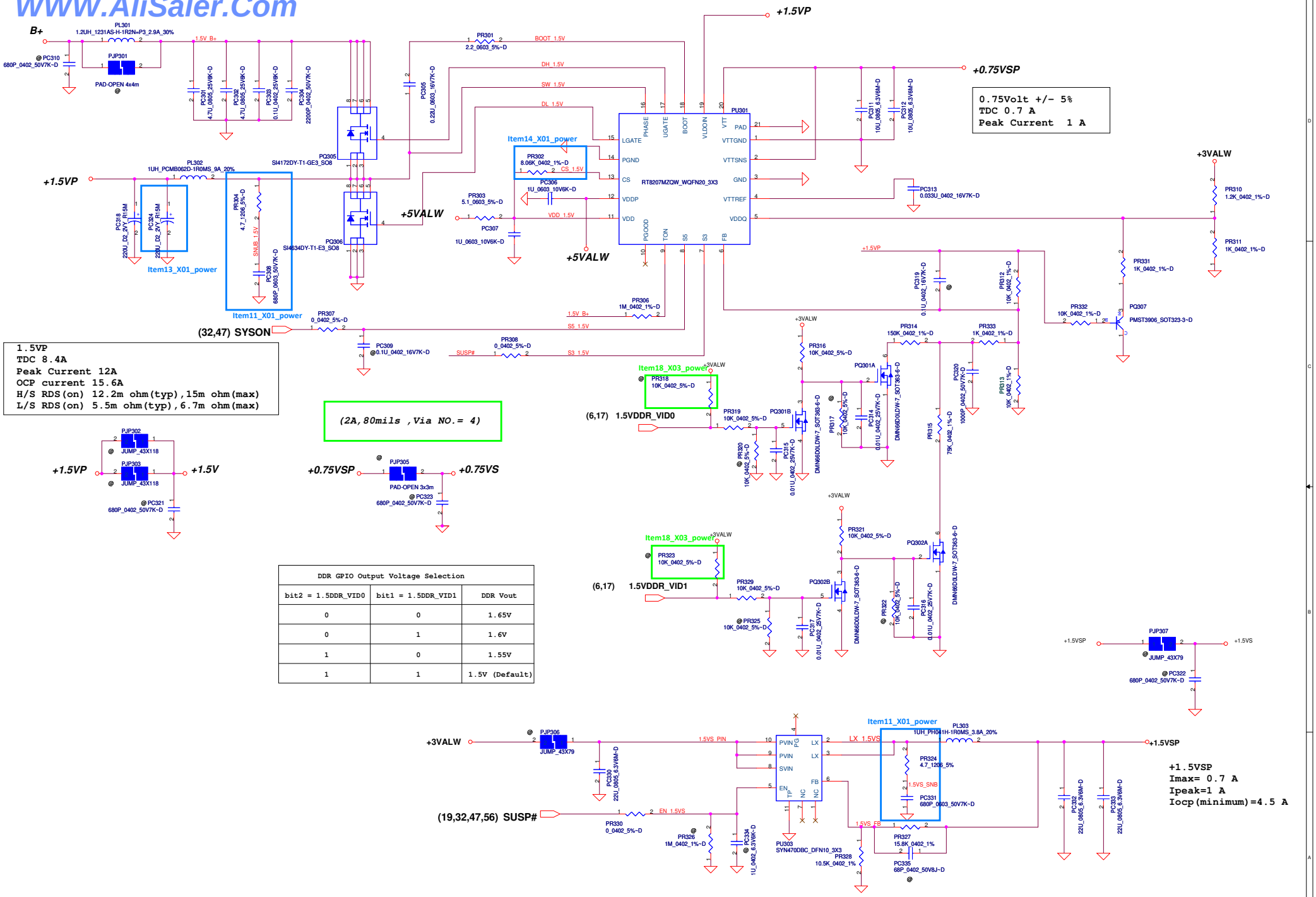
Security Classification	Compal Secret Data		
Issued Date	2011/01/31	Deciphered Date	2012/01/31

Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size	Document Number	Rev
Custom	LA-8381P	0.1

Date: Thursday, January 12, 2012 Sheet 54 of 63



DDR GPIO Output Voltage Selection		
bit2 = 1.5DDR_VID0	bit1 = 1.5DDR_VID1	DDR Vout
0	0	1.65V
0	1	1.6V
1	0	1.55V
1	1	1.5V (Default)

Security Classification	Compal Secret Data		
Issued Date	2011/01/31	Deciphered Date	2012/01/31

Compal Electronics, Inc.

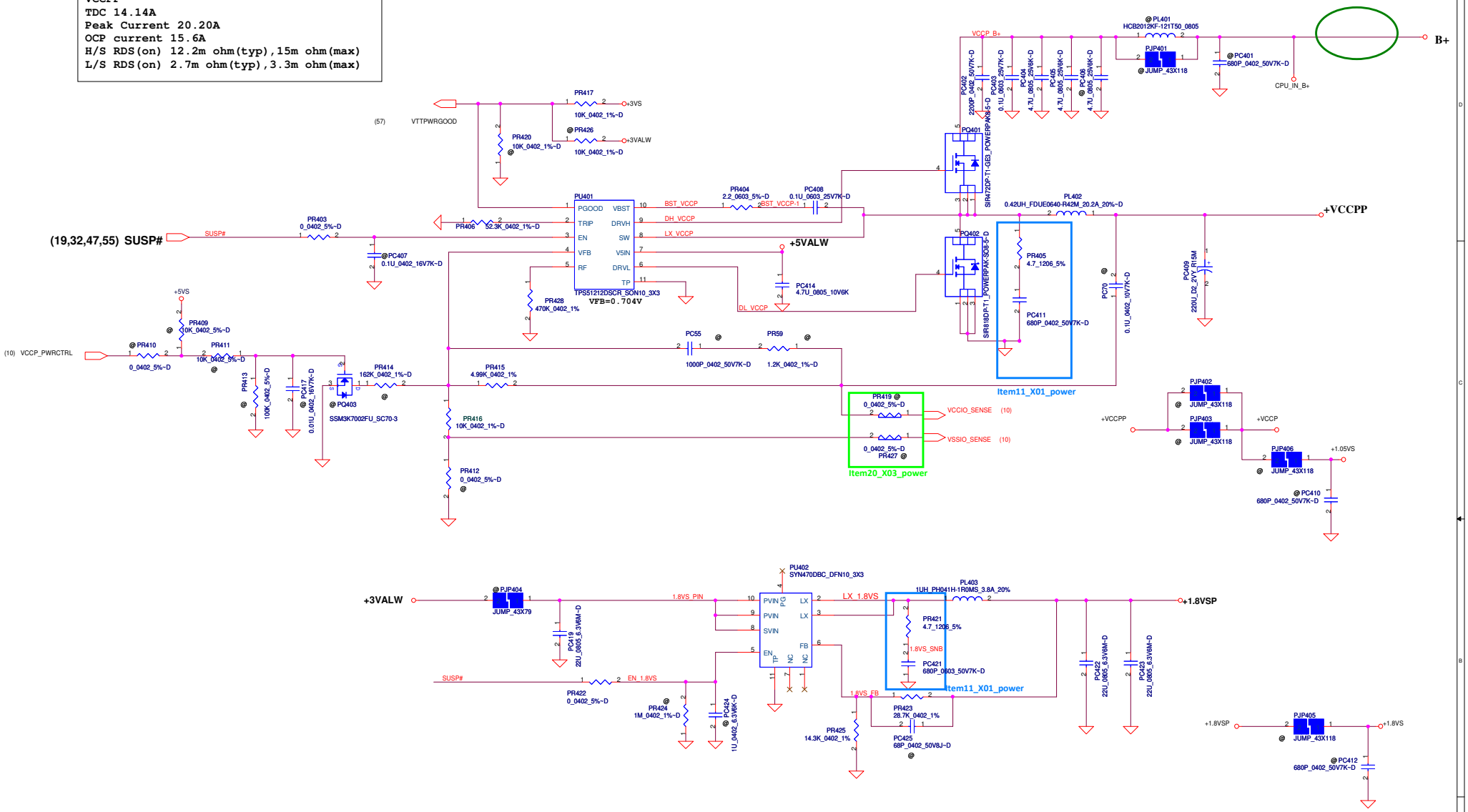
Title: 1.5VP/+0.75VSP/+1.5VSP

Size	Document Number	Rev
C	LA-8381P	0.1

Date: Thursday, January 12, 2012 Sheet 55 of 63

VCCPP
TDC 14.14A
Peak Current 20.20A
OCP current 15.6A
H/S RDS(on) 12.2m ohm(typ),15m ohm(max)
L/S RDS(on) 2.7m ohm(typ),3.3m ohm(max)

Due to remove VENTURA fun,
so delete PR401.



1.8VSP
TDC 1.08 A
Peak Current 1.55 A
OCP current 4.5 A

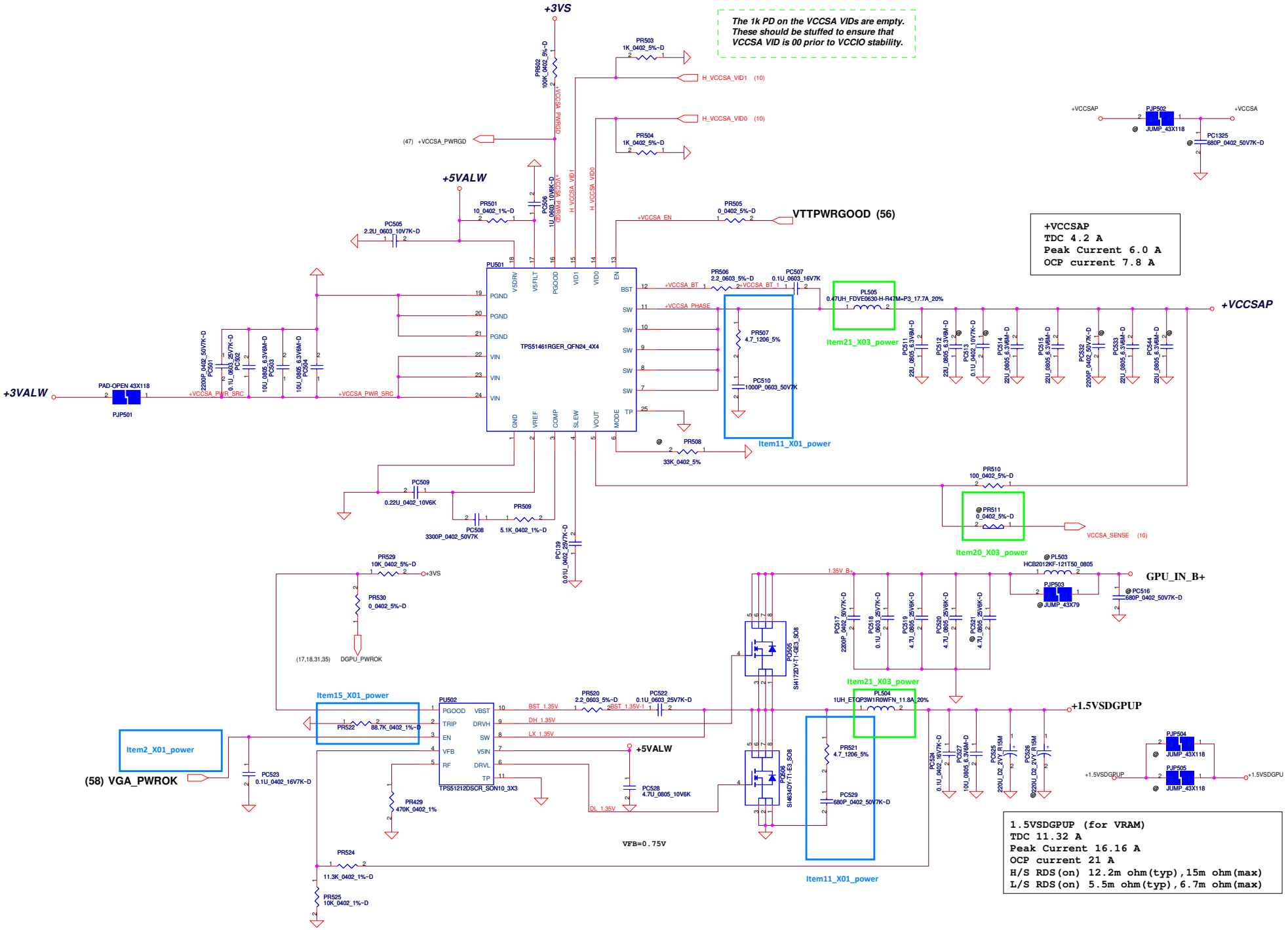
Security Classification	Compal Secret Data		
Issued Date	2011/01/31	Deciphered Date	2012/01/31

Compal Electronics, Inc.

Title: PWR+VCCPP/+1.8VSP

Size	Document Number	Rev
C	LA-8381P	1.0

Date: Thursday, January 12, 2012 Sheet 56 of 63



Security Classification	Compal Secret Data		
Issued Date	2011/01/31	Deciphered Date	2012/01/31

Compal Electronics, Inc.

Title: PWR-+VCCSAP/+1.5VSDGPUP

Size	Document Number	Rev
C	LA-8381P	0.1

Date: Thursday, January 12, 2012 | Sheet 57 of 63

N13P-GT
Initial voltage is 1.1V
EDP-TDC = 42 A
EDP-Peak = 60 A
OCP= 73.5 A
H/S RDS(on) 12.2m ohm(typ),15m ohm(max)
L/S*2 RDS(on) 2.7m ohm(typ),3.3m ohm(max)

Co-Lay
Item15_X02_power
PL714 HCB2012KF-121T50_0805
PL715 HCB2012KF-121T50_0805
Due to remove VENTURA fun, so delete PR601.
PAD-OPEN 43X118
PJP1101
GPU_IN_B+
B+

Item4_X01_power
Item1_X01_power
Item2_X01_power
Item6_X01_power
(31) DGPU_CORE_EN
PR650 10K_0402_5%~D
PC641 0.1U_0402_25V6K~D
PR660 2.2K_0402_5%~D
PR659 2.2K_0402_5%~D
PR661 2.2K_0402_5%~D
PR658 2.2K_0402_5%~D
PR662 2.2K_0402_5%~D
PR657 2.2K_0402_5%~D
PR663 2.2K_0402_5%~D
PR656 2.2K_0402_5%~D
PR664 2.2K_0402_5%~D
PR655 2.2K_0402_5%~D
PR665 2.2K_0402_5%~D
PR654 2.2K_0402_5%~D
PR653 2.2K_0402_5%~D
PR652 2.2K_0402_5%~D
GPU_VID_0
GPU_VID_1
GPU_VID_2
GPU_VID_3
GPU_VID_4
GPU_VID_5
H_DPRSLPVR
GPIO10_FBCREF_PSI#
+3VS

PR648 2.2K_0402_5%~D
(22) H_DPRSLPVR
PR651 2.2K_0402_5%~D
PR646 1.91K_0402_1%
CLK_ENABLE# VGA
PR644
PR669 0_0402_5%~D 10K_0402_5%~D
(57) VGA_PWROK
Item2_X01_power
PR642 47K_0402_1%~D
PR641 68_0402_5%~D
+VCCP
PR668 2.2K_0402_5%~D
PR667 @ 0_0402_5%~D
PR639 27.4K_0402_1%
PR638 @ 4.02K_0402_1%~D
VR_TT#
PH602 @ 470KB_0402_5%_ERTJ0EV474J
PC637 @ 22P_0402_50V8J~D
PR634 499_0402_1%~D
PC635 470P_0402_50V7K~D
PR635 3.57K_0402_1%~D
PC633 68P_0402_50V8J~D
PC648 150P_0402_50V8J~D
PR632 24K_0402_1%~D
PR637 @ 24K_0402_1%
PR636 @ 8.06K_0402_1%~D
PC636 100P_0402_50V7K~D
ISEN3_VGA
ISEN2_VGA
ISEN1_VGA
PC632 0.22U_0402_10V4Z
PC631 0.22U_0402_10V4Z
PC630 0.22U_0402_10V4Z
VSUM-_VGA
+VGA_CORE
PR625 @ 100_0402_5%~D
(23) VCCSENSE_VGA
PR626 @ 0_0402_5%~D
PC629 330P_0402_50V7K~D
Item20_X03_power
(23) VSSSENSE_VGA
PR627 @ 0_0402_5%~D
PC628 1000P_0402_50V7K~D
PR628 @ 100_0402_5%~D
PR634 82.5_0402_5%
PC627 @ 0.01U_0402_25V7K
PC626 0.22U_0603_10V7K~D
PR620 2.61K_0402_1%~D
PC625 4.7U_0603_10V6K~D
PR621 11K_0402_1%
PH601 10K_0402_5%_ERTJ0ER103J
PR623 698_0402_1%
PC622 0.1U_0402_16V7K~D
VSUM+_VGA
VSUM-_VGA

PU601 ISL62883CHRTZ-T_TQFN40_5X5
CLK_EN# DPRSLPVR VR_ON VID5 VID4 VID3 VID2 VID1 VID0
PGOOD PSI# RBIAS VR_TT# NTC VW COMP FB ISEN3 ISEN2 AGND
BOOT2 UGATE2 PHASE2 VSSP2 LGATE2 VCCP PWM3 LGATE1 VSSP1 PHASE1
ISEN1 VSEN RTN FCCM SUM+ SUM- VDD MON BOOT1 UGATE1
PC639 1U_0603_10V6K~D
PC638 1U_0603_10V6K~D
PR647 @ 0_0402_5%~D
PR631 0_0402_5%~@
Item20_X03_power
Item14_X02_power
PR1126 @ 0_0402_5%~D
PR629 @ 0_0402_5%~D
PR630 1_0402_5%
Item5_X01_power
PC624 1U_0603_10V6K~D
PC623 0.22U_0603_25V7K~D
Item20_X03_power

PU602 ISL6208CRZ-T_QFN8~D
VCC BOOT FCCM UGATE PWM PHASE GND LGATE
PC640 1U_0603_10V6K~D
PR608 2.2_0603_5%~D
PC618 0.22U_0603_10V7K~D
BOOT3 UGATE3_VGA PHASE3_VGA LGATE3_VGA

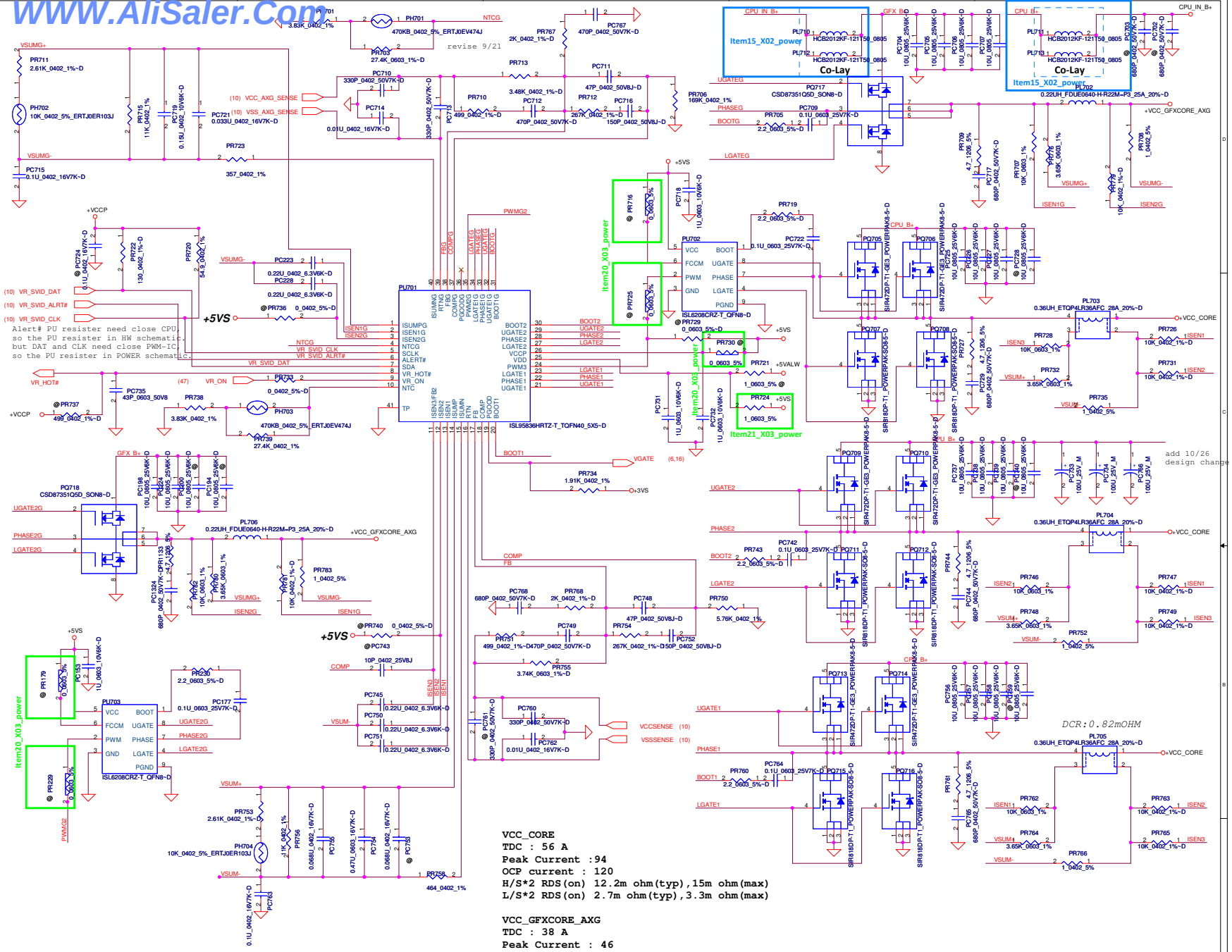
BOOT2_VGA
PR602 2.2_0603_5%~D
BOOT2_2_VGA
PC616 0.22U_0603_10V7K~D
UGATE2_VGA
PHASE2_VGA
LGATE2_VGA
PQ601 SIR472DP-T1-GE3_POWERPAK8-5~D
PQ602 PQ603 SIR818DP-T1_POWERPAK-SO8-5~D
PC601 2200P_0402_50V7K~D
PC602 PC603 PC604 PC605 4.7U_0805_25V6K~D
PR603 4.7_1206_5%
PC617 680P_0603_50V7K~D
PR604 3.48K_0402_1%
PR605 10K_0402_5%~D
V2P_VGA
V2N_VGA
VSUM+_VGA
VSUM-_VGA
ISEN2_VGA
ISEN3_VGA
ISEN1_VGA
PR1127 10K_0402_5%~D
PR1128 10K_0402_5%~D
PR607 1_0402_5%
PC642 PC643 470U_D2_2VM_R45M~D
PL602 0.22UH_FDUE0640-H-R22M=P3_25A_20%~D
+VGA_CORE
Item11_X01_power

PQ607 SIR472DP-T1-GE3_POWERPAK8-5~D
PQ608 PQ609 SIR818DP-T1_POWERPAK-SO8-5~D
PC606 2200P_0402_50V7K~D
PC607 PC608 PC609 PC610 4.7U_0805_25V6K~D
PR609 4.7_1206_5%
PC619 680P_0603_50V7K~D
PR610 3.48K_0402_1%
PR611 10K_0402_5%~D
V3P_VGA
V3N_VGA
PR1129 10K_0402_5%~D
PR1130 10K_0402_5%~D
PR613 1_0402_5%
PC644 PC645 470U_D2_2VM_R45M~D
PL604 0.22UH_FDUE0640-H-R22M=P3_25A_20%~D
+VGA_CORE
Item11_X01_power

PHASE1_VGA
UGATE1_VGA
LGATE1_VGA
PQ604 SIR472DP-T1-GE3_POWERPAK8-5~D
PQ605 PQ606 SIR818DP-T1_POWERPAK-SO8-5~D
PC611 2200P_0402_50V7K~D
PC612 PC613 PC614 PC615 4.7U_0805_25V6K~D
PR614 2.2_0603_5%~D
BOOT1_1_VGA
PC620 0.22U_0603_10V7K~D
PR615 4.7_1206_5%
PC621 680P_0603_50V7K~D
PR616 3.65K_0402_1%
PR617 10K_0402_5%~D
V1P_VGA
V1N_VGA
PR1131 10K_0402_5%~D
PR1132 10K_0402_5%~D
PR619 1_0402_5%
PC646 PC647 470U_D2_2VM_R45M~D
PL603 0.22UH_FDUE0640-H-R22M=P3_25A_20%~D
+VGA_CORE
Item11_X01_power

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.
Title: VGA_CORE
Size: C | Document Number: LA-XXXX | Rev: 0.1
Date: Thursday, January 12, 2012 | Sheet 58 of 63



Security Classification	Compal Secret Data		
Issued Date	2011/01/31	Deciphered Date	2012/01/31

Title: PWR-CPU_CORE

Size	Document Number	Rev
Custom	LA-8381P	0.2

Date: Thursday, January 12, 2012 Sheet 59 of 63

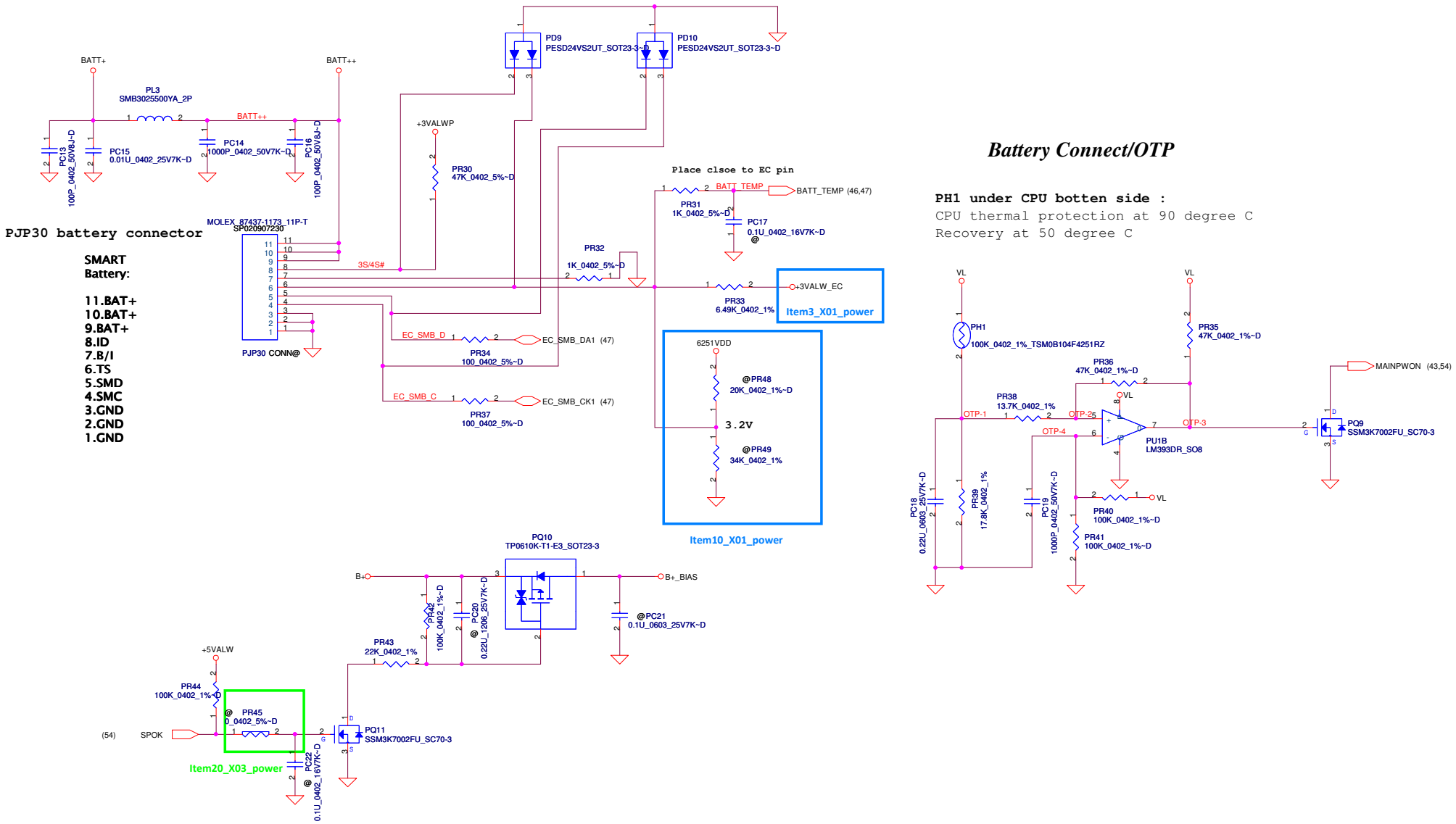
Battery Connect/OTP

PH1 under CPU botten side :
CPU thermal protection at 90 degree C
Recovery at 50 degree C

PJP30 battery connector

SMART Battery:

11.BAT+
10.BAT+
9.BAT+
8.ID
7.B/I
6.TS
5.SMD
4.SMC
3.GND
2.GND
1.GND



Security Classification	Compal Secret Data		
Issued Date	2011/01/31	Deciphered Date	2012/01/31

Compal Electronics, Inc.			
Title	PWR-BATTERY CONN		
Size: Custom	Document Number: LA-8381P		Rev: 0.1
Date: Thursday, January 12, 2012	Sheet 60 of 63		

+VCC_CORE

+VCC_CORE

PC1206 10U_0805_6.3V6M~D
PC1207 10U_0805_6.3V6M~D
PC1208 10U_0805_6.3V6M~D
PC1209 10U_0805_6.3V6M~D
PC1210 10U_0805_6.3V6M~D
PC1211 10U_0805_6.3V6M~D
PC1212 10U_0805_6.3V6M~D
PC1213 10U_0805_6.3V6M~D
PC1214 10U_0805_6.3V6M~D
PC1215 10U_0805_6.3V6M~D
@PC1216 10U_0805_6.3V6M~D

+VCC_CORE

PC1217 22U_0805_6.3V6M~D
PC1218 22U_0805_6.3V6M~D
PC1219 22U_0805_6.3V6M~D
PC1220 22U_0805_6.3V6M~D
PC1221 22U_0805_6.3V6M~D
PC1222 22U_0805_6.3V6M~D
PC1223 22U_0805_6.3V6M~D
PC1224 22U_0805_6.3V6M~D
PC1225 22U_0805_6.3V6M~D
PC1226 22U_0805_6.3V6M~D
PC1227 22U_0805_6.3V6M~D
PC1228 22U_0805_6.3V6M~D
PC1229 22U_0805_6.3V6M~D
PC1230 22U_0805_6.3V6M~D
PC1231 22U_0805_6.3V6M~D
PC1232 22U_0805_6.3V6M~D
@PC1233 22U_0805_6.3V6M~D
@PC1234 22U_0805_6.3V6M~D
@PC1235 22U_0805_6.3V6M~D

+VCC_CORE

PC1200 470U_D2_2VM_R4.5M~D
PC1201 470U_D2_2VM_R4.5M~D
PC1202 470U_D2_2VM_R4.5M~D
PC1203 470U_D2_2VM_R4.5M~D
PC1204 470U_D2_2VM_R4.5M~D
@PC1205 470U_D2_2VM_R4.5M~D
@PC1254 470U_D2_2VM_R4.5M~D
@PC1255 470U_D2_2VM_R4.5M~D

+VCC_GFXCORE_AXG

+VCC_GFXCORE_AXG

PC1236 22U_0805_6.3V6M~D
PC1237 22U_0805_6.3V6M~D
PC1238 22U_0805_6.3V6M~D
PC1239 22U_0805_6.3V6M~D
PC1240 22U_0805_6.3V6M~D
PC1241 22U_0805_6.3V6M~D
PC1242 22U_0805_6.3V6M~D
PC1243 22U_0805_6.3V6M~D
PC1244 22U_0805_6.3V6M~D
PC1245 22U_0805_6.3V6M~D
PC1246 22U_0805_6.3V6M~D
PC1247 22U_0805_6.3V6M~D
@PC1248 22U_0805_6.3V6M~D
@PC1249 22U_0805_6.3V6M~D
@PC1250 22U_0805_6.3V6M~D
@PC1251 22U_0805_6.3V6M~D
PC1253 470U_D2_2VM_R4.5M~D
PC1252 470U_D2_2VM_R4.5M~D

+VGA_CORE

+VGA_CORE

Under GPU

PC1296 0.1U_0402_10V7K~D
PC1295 0.1U_0402_10V7K~D
PC1294 0.1U_0402_10V7K~D
PC1293 0.1U_0402_10V7K~D
PC1304 4.7U_0603_6.3V6K~D
PC1303 4.7U_0603_6.3V6K~D
PC1302 4.7U_0603_6.3V6K~D
PC1301 4.7U_0603_6.3V6K~D
PC1300 4.7U_0603_6.3V6K~D
PC1299 4.7U_0603_6.3V6K~D
PC1298 4.7U_0603_6.3V6K~D
PC1297 4.7U_0603_6.3V6K~D
PC1309 4.7U_0603_6.3V6K~D
PC1308 4.7U_0603_6.3V6K~D
PC1307 4.7U_0603_6.3V6K~D
PC1306 4.7U_0603_6.3V6K~D
PC1305 4.7U_0603_6.3V6K~D
PC1322 4.7U_0603_6.3V6K~D
PC1323 4.7U_0603_6.3V6K~D

Below is 458544_CRV_PDDG_0.8 Table 5-6.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites

+VCCP

+VCCP

PC1266 22U_0805_6.3V6M~D
PC1265 22U_0805_6.3V6M~D
PC1264 22U_0805_6.3V6M~D
PC1263 22U_0805_6.3V6M~D
PC1262 22U_0805_6.3V6M~D
PC1261 22U_0805_6.3V6M~D
PC1260 22U_0805_6.3V6M~D
PC1259 22U_0805_6.3V6M~D
PC1258 22U_0805_6.3V6M~D
@PC1257 22U_0805_6.3V6M~D
PC1256 22U_0805_6.3V6M~D
PC1285 22U_0805_6.3V6M~D
PC1286 22U_0805_6.3V6M~D
PC1287 22U_0805_6.3V6M~D
PC1280 22U_0805_6.3V6M~D
PC1283 22U_0805_6.3V6M~D
PC1284 22U_0805_6.3V6M~D
PC1281 22U_0805_6.3V6M~D
PC1282 22U_0805_6.3V6M~D
PC1278 22U_0805_6.3V6M~D
@PC1288 22U_0805_6.3V6M~D
PC1279 22U_0805_6.3V6M~D
@PC1274 22U_0805_6.3V6M~D
@PC1272 22U_0805_6.3V6M~D
PC1271 22U_0805_6.3V6M~D
PC1270 22U_0805_6.3V6M~D
@PC1269 22U_0805_6.3V6M~D
PC1268 22U_0805_6.3V6M~D
@PC1267 22U_0805_6.3V6M~D
@PC1276 330U_D2_2VM_R6M~D
PC1275 330U_D2_2VM_R6M~D

+VGA_CORE

+VGA_CORE

Near GPU

@PC1315 330U_D2_2VM_R6M~D
PC1314 4.7U_0805_6.3V6M~D
PC1313 22U_0805_6.3V6M~D

PC1315 need ot close Power's phase 1

PC1321 4.7U_0603_6.3V6K~D
PC1320 4.7U_0603_6.3V6K~D
PC1319 4.7U_0603_6.3V6K~D
PC1318 4.7U_0603_6.3V6K~D
PC1317 4.7U_0603_6.3V6K~D

Security Classification	Compal Secret Data		
Issued Date	2008/09/15	Deciphered Date	2009/09/15

Compal Electronics, Inc.

Title: PWR - PROCESSOR DECOUPLING

Size	Document Number	Rev
	LA-8381P	0.1

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	61	PROCESSOR DECOUPLIN	11/09/9	COMPAL	Based on NVIDA check data to reduce VGA cap Q'ty	Remove PC1290~PC1293, PC1310,PC1312, PC1316.	0.1
2	55					Add PC1322, PC1323	0.1
3	58	+VGA_CORE	11/09/9	COMPAL	EE request	Add H_DPRSLPVR module port	0.1
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Compal Electronics, Inc.		
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Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

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Title: HW-PIR

Size	Document Number	Rev
		1.0

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